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Harmonizing power systems with a 13-level modified Packed U-Cells multi-level inverter: Design and implementation

Sherouk Fouda [a], Marwa S. Salem [b,c], Ahmed Saeed [d], Ahmed Shaker [e,*], M. Abouelatta [f], M. Abou El-Ela [d]

[a] Biomedical Engineering Department, Future University in Egypt, Cairo, Egypt
[b] Computer Engineering Department, College of Computer Science and Engineering, University of Ha'il, Ha'il, Saudi Arabia
[c] Electrical Communication and Electronics Systems Engineering Department, Faculty of Engineering, Modern Science and Arts University (MSA), Cairo, Egypt
[d] Electrical Engineering Department, Future University in Egypt, Cairo, Egypt
[e] Engineering Physics and Mathematics Dept., Ain Shams University, Cairo 11517, Egypt
[f] Electronics and Electrical Communications Dept., Ain Shams University, Cairo 11517, Egypt

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ABSTRACT

Traditional multilevel inverter designs often face complexity challenges, prompting the need for a simplified solution. This study introduces and evaluates the performance of a Modified Packed U-Cells (MPUC) inverter in the realm of multilevel inverter technology. The study addresses challenges associated with conventional multilevel inverters and proposes the MPUC inverter as a solution to simplify the design complexity. The MPUC inverter, utilizing three DC sources and eight switches, presents a groundbreaking thirteen-level output waveform. The primary focus lies in assessing the inverter's performance in terms of Total Harmonic Distortion (THD) and output voltage. Utilizing MATLAB/Simulink, the inverter's performance is evaluated with and without Pulse Width Modulation (PWM) strategies. The results reveal a notable reduction in THD, from 26.25% to 9.91% post-filtering when PWM is not employed. Various multi-carrier Level-Shifted PWM strategies, including PDPWM, PODPWM, APODPWM, and COPWM, are explored to enhance output waveform smoothness and efficiency. Unequal Carrier strategies, specifically UEAPDPWM and UEAPODPWM, emerge as superior in THD management at different frequency ranges. The study further incorporates real-time hardware implementation of the proposed 13-level MPUC topology, highlighting the success of the UEAPD-PWM strategy in improving waveform quality. The research aims to establish a multilevel inverter design protocol meeting international standards and emphasizes the pivotal role of PWM techniques in enhancing waveform quality. This comprehensive evaluation contributes to advancing the field of multilevel inverter technology and sets a benchmark for future research in this domain.

1. Introduction

The global energy landscape is undergoing a significant transformation, with photovoltaic (PV) systems emerging as a pivotal alternative to traditional electricity generation sources like coal, hydro, and nuclear power. These PV systems are not only crucial for meeting contemporary energy demands but are also projected to play an increasingly dominant role in future electricity production [1]. Central to the effectiveness of PV systems is the technology of Maximum Power Point Tracking (MPPT). This technology, along with power converter topologies and their controls, is designed to optimize the extraction of power from PV systems. MPPT methods, such as traditional approaches like Perturb and Observe (P&O) and Incremental Conductance (IC), as well as advanced techniques involving Artificial Neural Networks (ANN), play a key role. These methods are especially effective under varying conditions like partial shading, enhancing the overall efficiency of PV systems [2–5]. In the realm of power conversion, two primary types of converters are integral: DC/DC and DC/AC converters. The DC/DC converters are essential for ensuring that PV arrays operate at their Maximum Power Point (MPP), thus maximizing efficiency. In contrast, DC/AC converters are responsible for converting the DC output into a sinusoidal AC output, facilitating the integration of PV systems

* Corresponding author.
E-mail address: ahmed.shaker@eng.asu.edu.eg (A. Shaker).

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Table 1
Comparative Analysis of Level-Shift Multicarrier-Based PWM Techniques: Assessing Voltage Quality, Efficiency, Control Complexity, and Hardware Compatibility with Inverters.

PWM Technique	Voltage Quality	Efficiency	Control Complexity	Compatibility with Inverter's Hardware
Phase Displacement (PD)	Good voltage quality with reduced THD makes it suitable for applications requiring high-quality output.	Generally efficient due to simpler modulation strategy.	Low to moderate complexity, easier to implement and manage.	Compatible with most standard inverter hardware without needing extensive modifications.
Phase Opposition Disposition (POD)	Effective in reducing specific lower-order harmonics and improving voltage quality.	Efficiency is generally good but slightly lower than PD due to more complex waveforms.	The system exhibits moderate complexity due to the need to invert alternate carrier waves.	Generally compatible with standard inverters but may require careful configuration for optimal performance.
Alternative Phase Opposition Disposition (APOD)	Similar to POD, it targets different harmonics, improving varied voltage quality.	Efficiency, comparable to POD, varies depending on the targeted harmonics.	The system has moderate complexity, similar to POD, but focuses on different harmonic characteristics.	Compatible with inverters, similar to POD, with attention needed for specific harmonic control.
Carrier Overlapping (CO)	It can lead to a more complex harmonic spectrum but allows for finer control over voltage waveform.	Potentially less efficient due to more complex waveform generation.	The system displays high complexity due to the overlapping of carrier waves and the requirement for precise control.	Requires more advanced inverter hardware capable of handling complex modulation strategies.

Table 2
Evaluating PWM Techniques: A comprehensive approach for optimal performance and compliance with application requirements.

PWM Technique	Principle	Complexity	Key Characteristics	Suitability
Phase Displacement (PD)	Multiple PWM signals are used with each signal phase-shifted relative to others, reducing the total harmonic distortion (THD) in the system.	Low to Moderate	- Involves phase-shifting multiple PWM signals. - Reduces Total Harmonic Distortion (THD) effectively. - Simpler control algorithm and hardware requirements.	Ideal for applications requiring simpler control and low THD, like multi-level inverters.
Phase Opposition Disposition (POD)	Inverts every other carrier wave, leading to PWM signals that are in phase opposition, effectively reducing certain harmonics.	Moderate	- Inverts alternate carrier waves for phase opposition. - Efficient in reducing specific lower-order harmonics. - Requires precise timing control.	Suitable for specific harmonic reduction with moderately complex control strategies.
Alternative Phase Opposition Disposition (APOD)	Carrier waves are arranged so that adjacent carrier waves are 180 degrees out of phase, offering different harmonic profiles compared to POD.	Moderate	- Adjacent carrier waves are 180 degrees out of phase. - Targets different harmonics compared to POD. - Similar complexity to POD.	Best for systems needing reduction of a different set of harmonics with moderate control complexity.
Carrier Overlapping (CO)	Involves overlapping multiple carrier waves, allowing for greater control over the modulation process and a more complex harmonic spectrum.	High	- Involves overlapping multiple carrier waves. - Offers finer control over the output waveform. - Can lead to a more complex harmonic spectrum.	Ideal for advanced applications requiring fine modulation control, such as high-precision variable frequency drives.

with the local grid and powering AC loads [6].

The Multilevel Inverter (MLI) has gained prominence in this context due to its ability to meet stringent power quality and rating requirements. MLIs offer several advantages, including low switching losses, high voltage operation capability, reduced electromagnetic interference (EMI), and high efficiency. However, they also present challenges, mainly due to the cost implications of their extensive semiconductor switch and gate-driver circuitry requirements [7,8].

Classical MLI topologies, such as the Neutral Point Clamped (NPC), Flying Capacitor (FC), and Cascaded H-Bridge (CHB), are selected based on specific application needs, balancing factors like power level, efficiency, and cost. Despite their advantages in harmonics reduction and operational efficiency, these topologies often face issues of reliability and high costs [9]. MLIs are classified into three types: symmetrical, using equal DC voltage sources for simplicity; asymmetrical, employing varying voltage sources for more voltage levels and efficiency but with increased complexity; and hybrid, which blends both to optimize performance and component usage. The primary objective of MLIs is to achieve a large number of output voltage steps, minimize total harmonic distortion (THD), and maximize efficiency. This design focus helps in enhancing power quality and operational efficiency in various applications. MLIs like the NPC, FC, and CHB use high-frequency switches to improve performance, enabling seamless grid connections and balanced load distribution. This results in high-quality output waveforms, reduced switch stress, and lower electromagnetic interference, making MLIs ideal for PV power inverters and diverse inverter applications [7, 10–12]. Despite their effectiveness in enhancing harmonics, the NPC, FC, and CHB topologies of MLIs often face issues with reliability and high costs, primarily due to the extensive use of switches and capacitors in their design. To address these challenges, recent research has concentrated on minimizing the size and cost of MLI systems, primarily through reducing the number of components required.

In response to these challenges, recent developments have introduced in 2011 the Packed U-Cells (PUC) inverter [13], a novel MLI topology aimed at reducing component count, thereby enhancing efficiency and reducing costs. This topology provides very high levels of

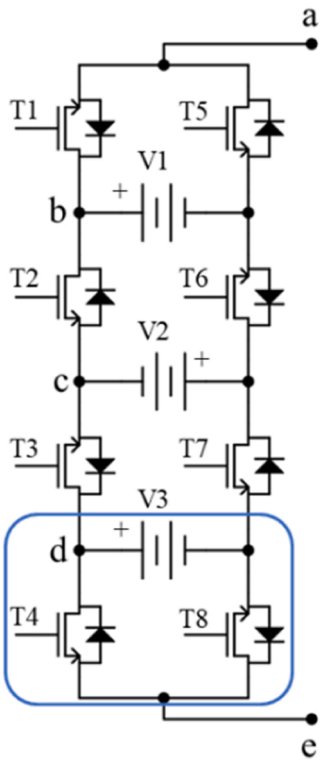


Fig. 1. Thirteen-level MPUC inverter topology.

efficiency without the use of numerous semiconductor-based switching devices and capacitors. For instance, six switches (IGBTs), one DC power source, and one electrolytic capacitor, used as an auxiliary DC power source, are used in the case of the 7-PUC inverter [13]. Additionally, adding one capacitor and two switches to the PUC inverter allows for the generation of two additional voltage levels [14].

To control MLIs, various switching techniques are employed, including carrier-based methods, selective harmonic elimination, and space vector modulation. The predominant control method is multicarrier-based Pulse Width Modulation (PWM), appreciated for its simplicity and effectiveness in reducing THD in output voltage. Carrier-based PWM typically utilizes a triangular carrier waveform for its superior harmonic characteristics in MLI outputs. The control of MLIs is predominantly managed through Level-shift multicarrier-based PWM techniques. These techniques, including Phase Displacement (PD), Phase Opposition Disposition (POD), Alternative Phase Opposition Disposition (APOD), and Carrier Overlapping (CO), are essential in balancing voltage quality, efficiency, control complexity, and hardware compatibility [15,16]. Table 1 summarizes the Level-shift multi-carrier-based PWM techniques regarding voltage quality, efficiency, control complexity, control complexity, and compatibility with the inverter's hardware.

A comprehensive evaluation based on four key categories is essential in selecting a PWM technique. The first factor, harmonic performance, involves evaluating the PWM technique's power quality management and regulatory compliance, focusing on reducing specific harmonics and keeping THD within acceptable limits for sensitive equipment or power grids. Control strategy complexity requires analyzing the intricacies of the PWM technique, which encompasses the complexity of its circuitry and control algorithms, the necessity for real-time control adjustments, and the effects these have on resources and costs. Application-specific requirements focus on meeting the unique demands of different applications, encompassing factors like efficiency levels, switching frequencies, heat dissipation, power quality for sensitive loads, and compliance with EMI and power quality standards. Finally, efficiency and reliability ensure that the PWM method is both efficient in power conversion and dependable, crucial for high-performance applications such as renewable energy systems or electric vehicles. Overall, selecting a PWM technique requires a detailed and balanced evaluation of these considerations, tailored to the specific needs and limitations of the intended application as shown in Table 2. This comprehensive approach ensures that each aspect of the PWM technique is aligned with the

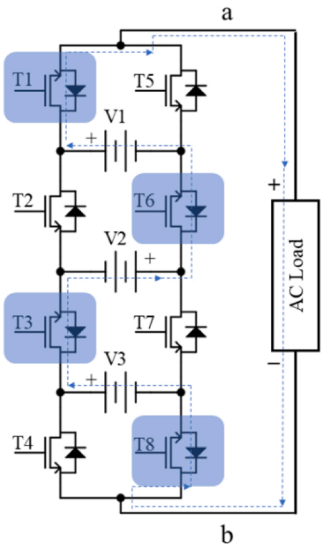


Fig. 2. The first working state of the thirteen-level MPUC topology.

Table 3
Switching States and The Desired Thirteen Voltage Levels That Produced by 13-MPUC.

Modes	Switching Sequence									
	State numeral	T1	T2	T3	T4	T5	T6	T7	T8	Value
Positive Levels	1	1	0	1	0	0	1	0	1	$V_1 + V_2 + V_3$
	2	1	0	1	1	0	1	0	0	$V_1 + V_2$
	3	0	0	1	0	1	1	0	1	$V_2 + V_3$
	4	1	1	1	0	0	0	0	1	V_3
	5	0	0	1	1	1	1	0	0	V_2
	6	1	0	0	0	0	1	1	1	V_1
Zero Level	7	0	0	0	0	1	1	1	1	0
	7'	1	1	1	1	0	0	0	0	0
Negative Levels	8	0	1	1	1	1	0	0	0	$-V_1$
	9	1	1	0	0	0	0	1	1	$-V_2$
	10	0	0	0	1	1	1	1	0	$-V_3$
	11	1	1	0	1	0	0	1	0	$-(V_2 + V_3)$
	12	0	1	0	0	1	0	1	1	$-(V_1 + V_2)$
	13	0	1	0	1	1	0	1	0	$-(V_1 + V_2 + V_3)$

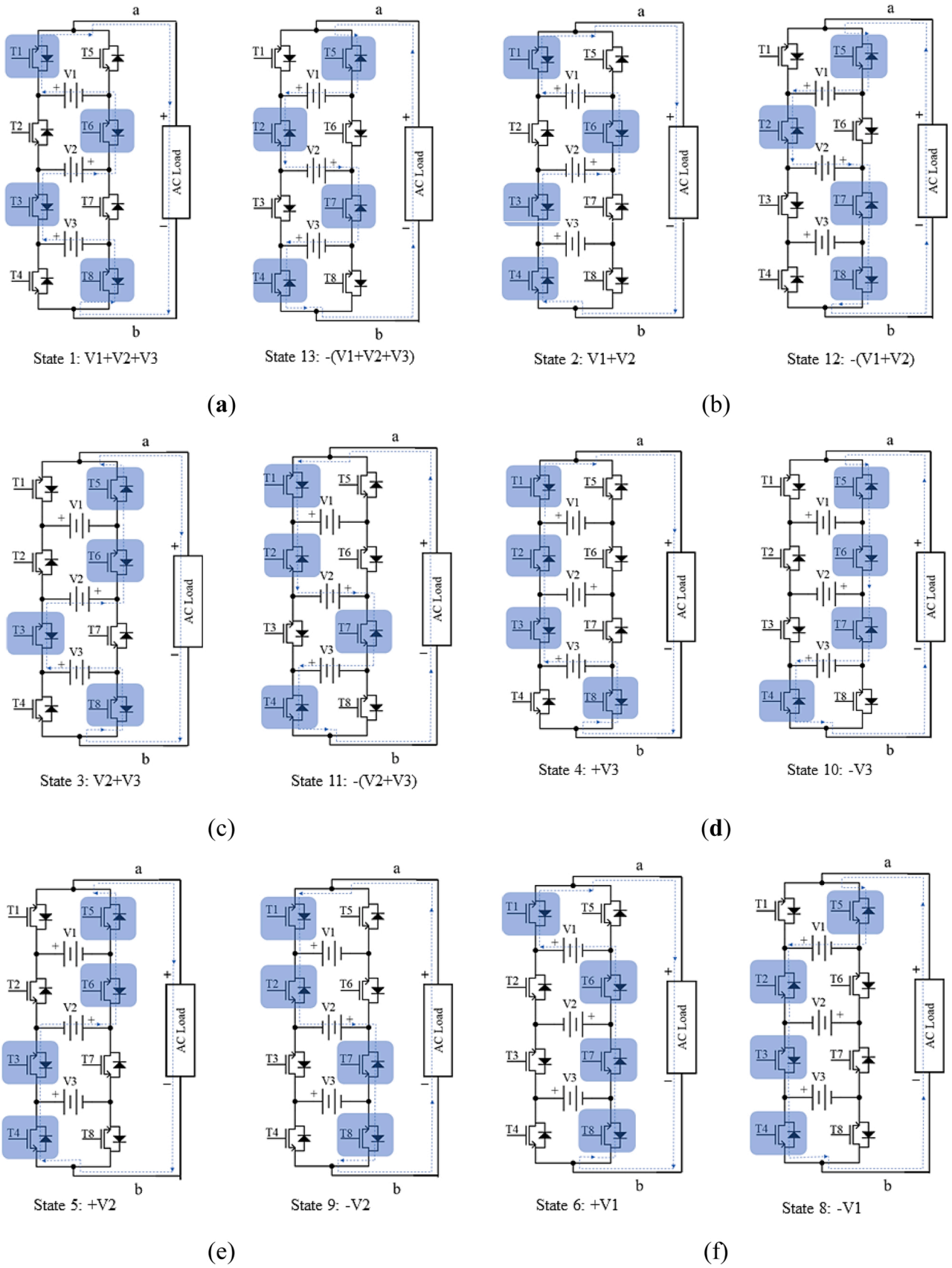


Fig. 3. The operation of six positive states and their corresponding opposite six negative states of 13-level MPUC Voltages (a) State 1: $+(V_1+V_2+V_3)$, State 13: $-(V_1+V_2+V_3)$. (b) State 2: $+(V_1+V_2)$, State 12: $-(V_1+V_2)$. (c) State 3: $+(V_2+V_3)$, State 11: $-(V_2+V_3)$. (d) State 4: $+V_3$, State 10: $-V_3$. (e) State 5: $+V_2$, State 9: $-V_2$. (f) State 6: $+V_1$, State 8: $-V_1$.

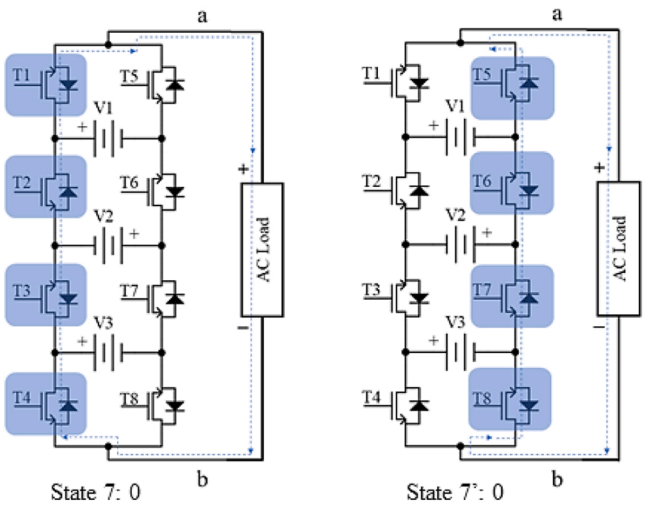


Fig. 4. The operation of zero states of 13-level MPUC Voltages.

application's requirements, resulting in optimal performance and compliance [16–18].

This work presents a modified Packed U-Cells thirteen-level multilevel inverter (13-MPUC) that aims to enhance voltage levels further and reduce THD using a limited number of power switches. Building upon the seven-level MPUC structure [19], this modification adds more switches to create 13 voltage levels. The advantages of the 13-level MPUC are manifold: it achieves higher peak voltage by utilizing three DC sources instead of a single DC source and two DC-link capacitors, allows for higher switching frequencies, simplifies control without the need for additional circuits to manage the charge/discharge of the DC-link capacitor, and effectively reduces THD. Furthermore, the proposed topology demonstrates the ability to create a 380 V inverter using 27 V PV panels through series strings of 4, 5, and 6 panels. In addition, we study the proposed thirteen-level MPUC inverter topology without and with a comprehensive comparison of various level-shifted multi--carrier PWM (LS-PWM) topologies with different frequencies, focusing on their impact on waveform quality. This analysis shows PWM's crucial role in improving the output waveform, which becomes more sine-wave-like after filtering, enhancing efficiency and effectiveness for any load. To comply with the IEEE519 standard [20] and achieve a THD of 5% or less, an LCL filter is integrated into the inverter, effectively reducing voltage and current harmonics. The inverter's performance without and with using LS-PWM techniques are evaluated through MATLAB/Simulink simulations. Additionally, real-time implementation of the 13-MPUC inverter is tested, both with and without the UEAPD-PWM technique, resulting in efficient performance.

The rest of the paper is structured as follows. The procedure of the proposed thirteen-level MPUC inverter topology is described in Section 2. Also, the difference between the presented topology and the 7-level MPUC is elucidated. Section 3 presents the discussion and the results of the simulation. Section 4 is devoted to the experimental results, while Section 5 compares the previous topologies and the proposed 13-MPUC topology regarding their component count and desired output levels. Finally, Section 6 provides some concluding remarks.

2. The proposed topology of thirteen-level MPUC

Herein, a modified multilevel inverter has been developed to enhance performance, specifically in terms of Total Harmonic Distortion (THD). The primary objective of this study is to establish a methodology for constructing a low THD step sine wave inverter that meets standard specifications. This will be achieved by adapting and redesigning the multilevel inverter configuration to increase the number of voltage levels and the output voltage, thus reducing THD.

The proposed topology enhances the seven-level MPUC structure introduced in [19] by using 8 switches instead of 6, converting the circuit into a 13-level MPUC [21]. The advantages of the 13-level MPUC can be summarized as follows:

1. A higher peak voltage can be achieved using the same DC sources.
2. THD is effectively decreased.
3. It is possible to build a 380 V_p inverter using PV panels of 27 V (V_{out}), where we can use series strings of 4, 5, and 6 panels to produce 108 V, 135 V, and 162, respectively.
4. Topology is used in the proposed 3 DC sources instead of a single DC source and DC-link capacitor. It makes the circuit commute at higher switching frequencies since the time needed to charge the DC-link capacitor is eliminated.
5. There is no need to add a control circuit, especially to control the charge/discharge of the DC-link capacitor; we only need to control the power switches in the circuit.

The MPUC inverter configuration exemplifies an effective blend of simplicity and cost-efficiency. With its ability to generate thirteen levels using only eight Insulated-Gate Bipolar Transistor (IGBT) switches and three distinct DC sources, it significantly reduces the reliance on capacitors. This design simplifies the control mechanisms and allows the flexible use of various PV module values to produce DC voltages independent of capacitors or diodes. Although the MPUC inverter incorporates advanced features, these do not necessarily translate into increased complexity or cost. Instead, its design efficiently balances sophisticated modulation techniques and the ability to handle fluctuating renewable energy sources without significantly complicating manufacturing and maintenance processes. These advanced components and technologies are integrated without markedly elevating production costs. It makes MPUC inverters a feasible and practical choice for diverse applications, especially in renewable energy systems.

The mentioned system represents a modified MLI configuration based on the PUC topology. It replaces the DC-link capacitors with separate DC sources to reduce control complexity. The system can generate seven voltage levels at its output using two sources of DC voltage and six IGBTs, employing the Multicarrier-based method to control the IGBTs. When three independent DC sources of $V_1 = 2\,V_2$ and $V_2 = 2\,V_3$ (i.e., $V_1 = 4\,V_3$) and eight IGBT switches are used in the proposed topology, the typical methodology described in the section results in a thirteen-level MPUC, as illustrated in Fig. 1. The summation of the DC sources V_1, V_2, and V_3 equals 7 V_3. There are asymmetrical steps in the output waveform to prevent a short circuit condition in the current path and produce the desired voltage levels. The conditions of the eight proposed IGBTs and their output desired voltage are represented in Table 3, which illustrates the different thirteen states.

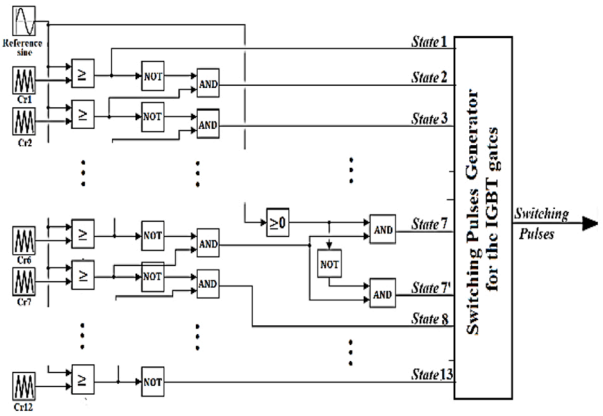
Furthermore, the various states can be clarified through Figs. 2, 3, and 4. Fig. 2 illustrates the way the first state operates. The negative half-cycle exhibits six working states, while the positive half-cycle involves the other six working states, as demonstrated in Fig. 3. An additional operating state is identified for the zero level, as illustrated in Fig. 4. Two redundant switching states are recognized for the zero Level, namely case 7 and case 7', chosen by the control circuitry.

Eqs. (1) and (2) define the ON-OFF function and the thirteen-MPUC inverter's output voltage, respectively, where S_i represents the desired switch.

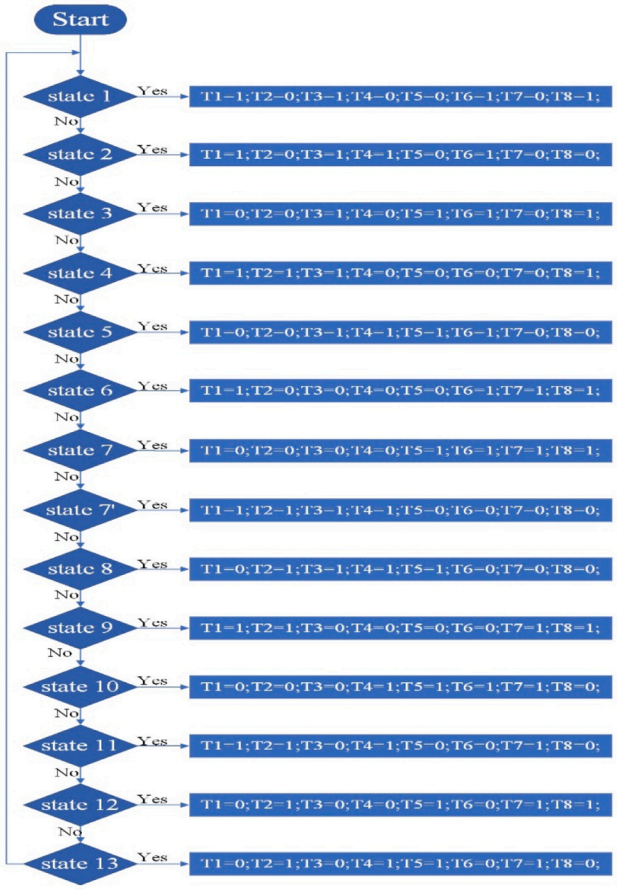
$$S_i = \begin{cases} 0 & if \quad S_i \quad is \quad OFF \\ 1 & if \quad S_i \quad is \quad ON \end{cases} \quad i = 1,2,3,4 \tag{1}$$

$$V_{ae} = V_{ab} + V_{bc} + V_{cd} + V_{de} \tag{2}$$

As outlined in Table 3, the switching function contributes to the computation of the voltage at each node that is demonstrated at the points a, b, c, d, and e:



(a)



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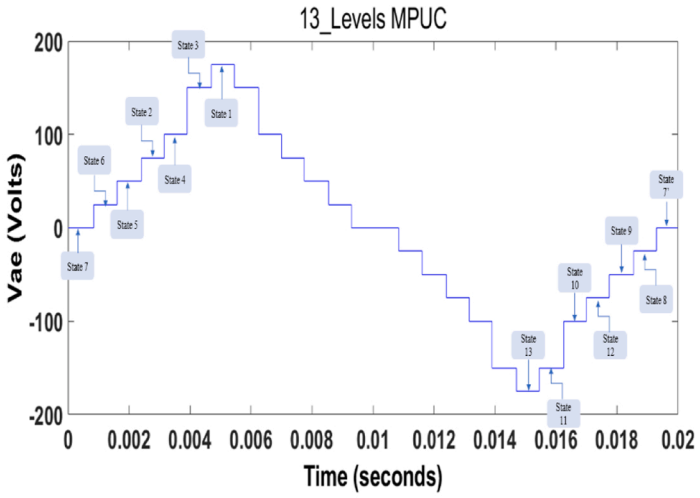

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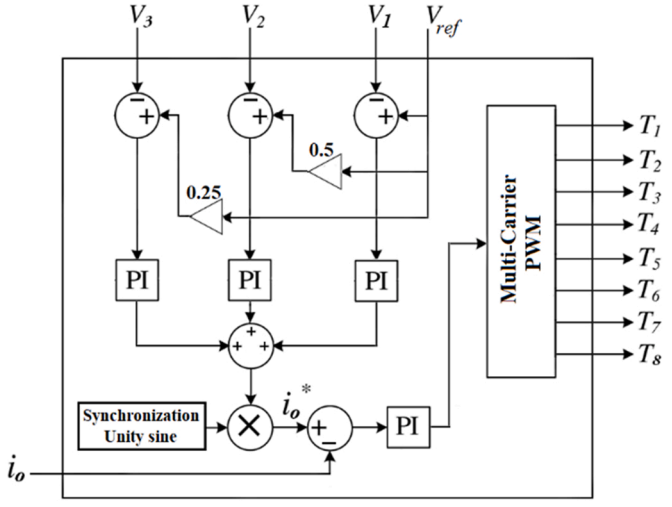


(d)

Fig. 5. (a) The generation of the ON-OFF switching states of the thirteen-level MPUC topology using Multi-carrier level-shifted PWM (LS-PWM). (b) Flowchart Illustrates the algorithm for determining IGBT gates' ON-OFF signals. (c). Voltage Levels and Corresponding Operational States in Output Waveforms. (d) The designed schematic of the inverter control.

$$\begin{aligned} \&V_{ab} &= V_1(S_1 - 1) \\ \&V_{bc} &= (V_1 + V_2)(1 - S_2) \\ \&V_{cd} &= (V_2 + V_3)(1 - S_3) \\ \&V_{de} &= V_3(1 - S_4) \end{aligned} \tag{3}$$

By substituting (3) into (2),

$$V_{ae} = (S_1 - S_2)V_1 + (2 - S_2 - S_3)V_2 + (2 - S_3 - S_4)V_3 \tag{4}$$

As stated above, V_1 is twice V_2, and V_2 is twice V_3 (i.e., $V_1 = 4\ V_3$). Eqs. 1, 2, 3, and 4 depict the optimal scenario where switches are coordinated to simultaneously conduct and achieve the summation of the three DC sources. This formulation emphasizes the synchronized operation of the switches to fulfill this objective. The common objective is to improve the PV system's performance and efficiency by maintaining the PV module at its maximum power operation.

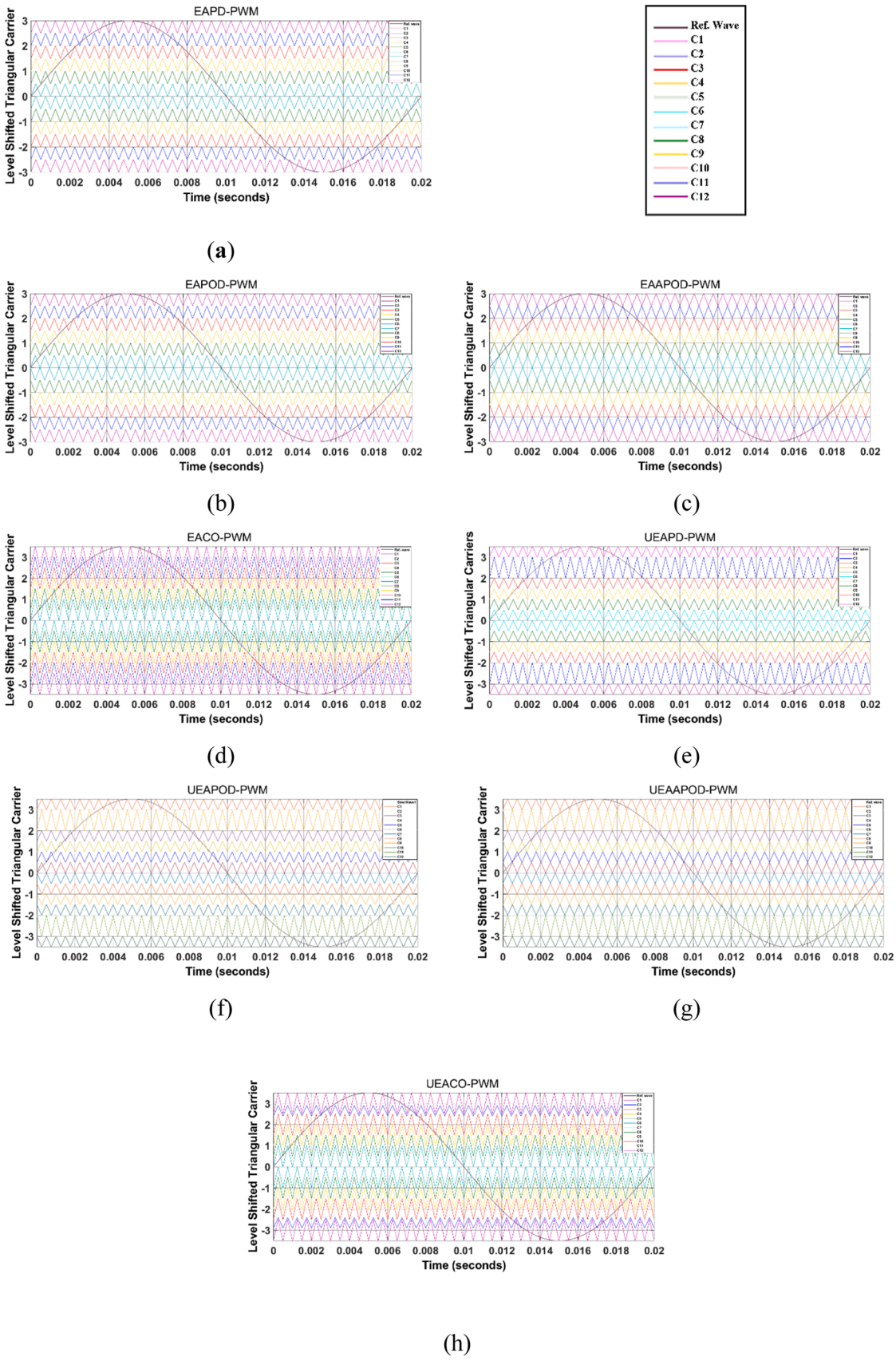


Fig. 6. (a) Multi-carrier EAPD-PWM for Thirteen-level Modified-PUC inverter. (b) Multi-carrier EAPOD-PWM for Thirteen-level Modified-PUC inverter. (c) Multi-carrier EAAPOD-PWM for Thirteen-level Modified-PUC inverter. (d) Multi-carrier EACO-PWM for Thirteen-level Modified-PUC inverter. (e) Multi-carrier UEAPD-PWM for thirteen-level Modified-PUC inverter. (f) Multi-carrier UEAPOD-PWM for Thirteen-level Modified-PUC inverter. (g) Multi-carrier UEAAPOD-PWM for Thirteen-level Modified-PUC inverter. (h) Multi-carrier UEACO-PWM for Thirteen-level Modified-PUC inverter.

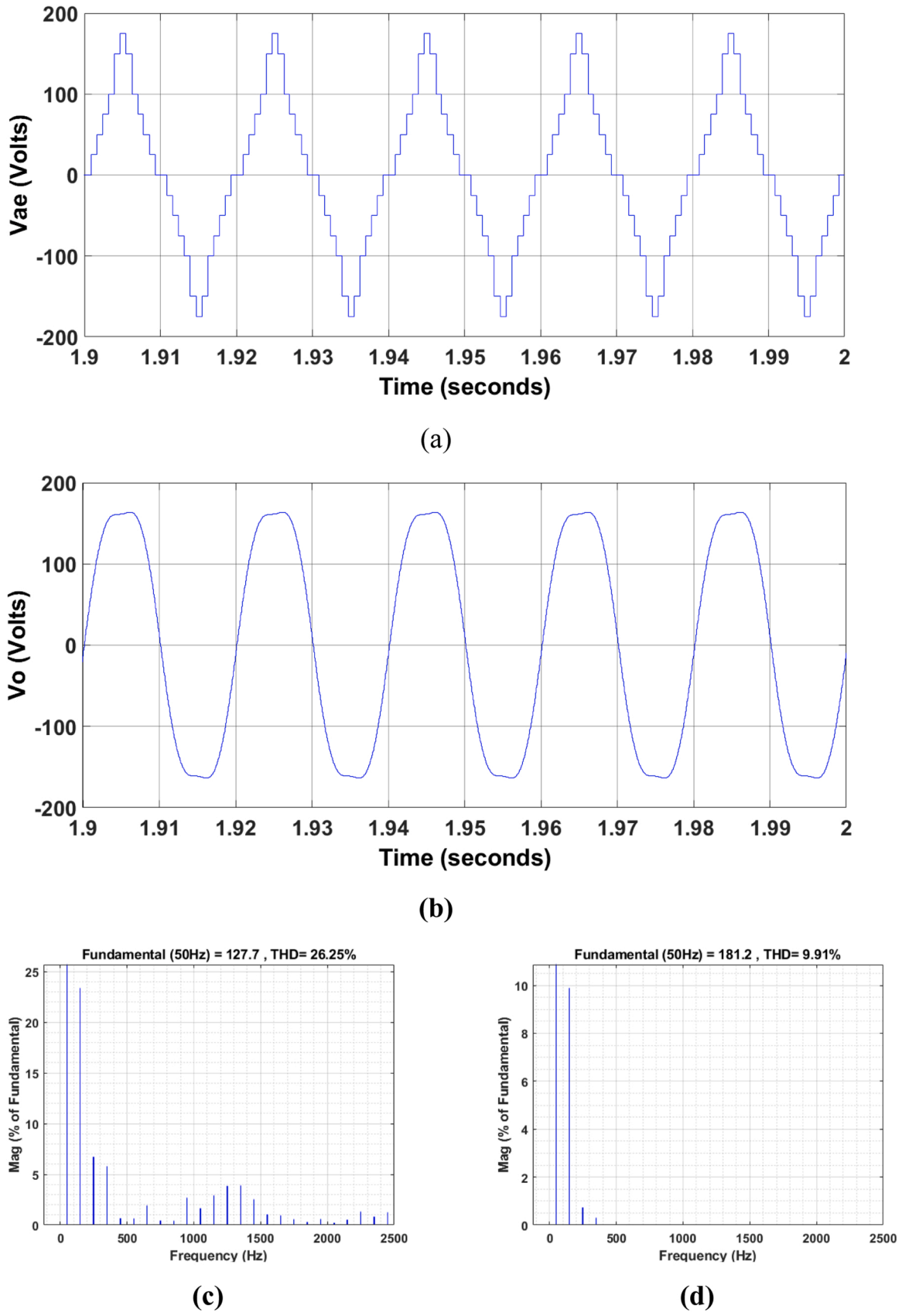


Fig. 7. **(a)**The proposed Thirteen-level MPUC output voltage waveform without the PWM technique before using the filter. **(b)**The proposed Thirteen-level MPUC output voltage waveform without the PWM technique after using the filter. **(c)**The THD of the proposed Thirteen-level MPUC output voltage waveform without the PWM technique before using the filter. **(d)**The THD of the proposed Thirteen-level MPUC output voltage waveform without the PWM technique after using the filter.

Table 4
Simulation Parameters of Thirteen Modified-PUC Inverter.

Parameters	Value
V_1	100 V
V_2	50 V
V_3	25 V
Resistive Load (R_L)	2 KΩ
Inductive Load (R, I_L)	2kΩ, 2.5 mH
Frequency of the Reference wave	50 Hz
Frequency of the Multi-carriers	2 kHz, 3.5 kHz, 4 kHz, 4.5 kHz, 5 kHz, 5.5 kHz, 8 kHz, 10 kHz
Load Change (at a time)	2 sec
Carriers Peak-to-peak Amplitude	25, 50 V
Amplitude modulation index: ma	1
Frequency modulation index: mf	40

3. Results of the proposed topology

3.1. Simulation results

The logic simulation employed to generate the switching states of the 13-MPUC is detailed in Fig. 5. This process begins in Fig. 5(a), with the generation of PWM using twelve carrier waves. Each carrier has a distinct amplitude matching the peak-to-peak amplitude of a 50 Hz sine wave. These carriers are compared against the sine wave, which has an amplitude of 175, to produce thirteen unique switching states. The process begins with the identification of switching states, as illustrated in Fig. 3, where each state is linked to a specific voltage level. These states are crucial for the operation of a switching pulse generator block, which employs a distinct algorithm for its functionality. The algorithm in question is detailed in a flowchart presented in Fig. 5(b). For a comprehensive understanding, Fig. 5(c) provides a circuit diagram that illustrates the operated switches in conjunction with the corresponding voltage levels previously outlined in Fig. 3 and Fig. 4. This sequence of figures collectively explains the implementation of the algorithm through the switching pulse generator block, highlighting the relationship between the switching states, voltage levels, and the operational circuit. The algorithm is critical for accurately determining the ON and OFF states of the 13-MPUC's eight switches, ensuring precise and efficient operation. This algorithm is key in controlling the switching states of the 13-MPUC, guaranteeing accurate and effective performance. Fig. 5(d) provides a detailed schematic of the custom-designed controller, engineered to achieve a thirteen-level harmonic structure with optimal quality. This figure demonstrates the technique for generating a reference sine wave by harnessing three discrete DC sources, a methodology commonly applied in scenarios involving PV modules or DC power systems. The amplitude of the sine wave is equal to the total voltage of the three DC sources combined, and it operates at a consistent frequency of 50 Hz. This sine wave is crucial for comparing various carriers to produce precise PWM pulses, essential in forming a reference waveform that meets the requirements for efficient PWM pulse generation.

To eliminate the DC voltage errors, i.e., V_1, V_2, and V_3, three proportional-plus-integral (PI) controllers are utilized. A unity-sine wave augmented the output voltage controller to serve as a reference current that must be produced at the O/P. A comparison is thus made between the reference current and the present output current. The PI-controller controls the comparison, which generates the reference sine regulated typically in the same way as the ON-OFF algorithm illustrated in Fig. 5(a) to derive the IGBT gates' ON-OFF signals.

One of the multilevel inverter's characteristic features is that the current harmonics are reduced in the load. Indeed, utilizing the control technique is responsible for enhancing the current spectrum. In this regard, it is noted that the most common control technique, utilizing

Table 5
THD% For Equal Amplitude of Carriers for Different Modulation Strategies Before Filtering Across Various Frequencies.

Modulation strategies	THD% 2 kHz	THD% 3.5 kHz	THD% 4 kHz	THD% 4.5 kHz	THD% 5 kHz	THD% 5.5 kHz	THD% 8 kHz	THD% 10 kHz
Equal carriers-PDPWM	9.62% with output voltage 170.8 V	9.62% with output voltage 170.9 V	10.36% with output voltage 170.1 V	10.16% with output voltage 171.4 V	11.16% with output voltage 169.2 V	10.12% with output voltage 171.8 V	11.46% with output voltage 170.8 V	19.69% with output voltage 167 V
Equal carriers-PODPWM	9.23% with output voltage 171 V	9.04% with output voltage 171 V	10.47% with output voltage 170.1 V	9.97% with output voltage 171.2 V	11.44% with output voltage 169.2 V	10.06% with output voltage 171.5 V	10.98% with output voltage 171.8 V	15.16% with output voltage 167 V
Equal carriers-APODPWM	8.98% with output voltage 171.1 V	9.10% with output voltage 171 V	9.28% with output voltage 171.5 V	10.22% with output voltage 171.5 V	11.03% with output voltage 169.3 V	9.56% with output voltage 172.1 V	10.91% with output voltage 171.5 V	15.40% with output voltage 166.9 V
Equal carriers-COPWM	13.97% with output voltage 174.4 V	14.29% with output voltage 175.2 V	13.60% with output voltage 175.7 V	14.56% with output voltage 175.2 V	16.69% with output voltage 173.4 V	14.91% with output voltage 175.7 V	15.41% with output voltage 174.4 V	29.52% with output voltage 168.9 V

Table 6
THD% For Unequal Amplitude of Carriers Different Modulation Strategies Before Filtering Across Various Frequencies.

Modulation strategies	THD% 2 kHz	THD% 3.5 kHz	THD% 4 kHz	THD% 4.5 kHz	THD% 5 kHz	THD% 5.5 kHz	THD% 8 kHz	THD% 10 kHz
Unequal carriers-PDPWM	8.81% with output voltage 173.4 V	8.52% with output voltage 174.9 V	9.19% with output voltage 174.6 V	8.44% with output voltage 175.1 V	10.39% with output voltage 173.5 V	8.93% with output voltage 175.4 V	11.35% with output voltage 173.4 V	20.79% with output voltage 170.5 V
Unequal carriers-PODPWM	9.44% with output voltage 172.5 V	7.87% with output voltage 175.7 V	9.13% with output voltage 176.2 V	8.24% with output voltage 175.7 V	10.21% with output voltage 173.7 V	9.01% with output voltage 175.1 V	11.09% with output voltage 174.4 V	16.02% with output voltage 170.3 V
Unequal carriers-APODPWM	8.59% with output voltage 173.8 V	8.98% with output voltage 174.8 V	8.85% with output voltage 174.7 V	8.57% with output voltage 175.4 V	9.62% with output voltage 172.8 V	8.66% with output voltage 175.3 V	10.81% with output voltage 173.7 V	16.08% with output voltage 171 V
Unequal carriers-COPWM	13.27% with output voltage 172.5 V	13.90% with output voltage 172.6 V	14.21% with output voltage 172.1 V	13.96% with output voltage 172.8 V	15.65% with output voltage 170.8 V	14.48% with output voltage 173 V	14.76% with output voltage 172.5 V	26.56% with output voltage 167 V

Table 7
THD% For Equal Amplitude of Carriers Different Modulation Strategies After Filtering Across Various Frequencies.

Modulation strategies	THD% 2 kHz	THD% 3.5 kHz	THD% 4 kHz	THD% 4.5 kHz	THD% 5 kHz	THD% 5.5 kHz	THD% 8 kHz	THD% 10 kHz
Equal carriers-PDPWM	3.80% with output voltage 242.5 V	2.65% with output voltage 242.7 V	2.23% with output voltage 241.5 V	2.37% with output voltage 243.4 V	1.91% with output voltage 240.2 V	2.52% with output voltage 243.9 V	2.37% with output voltage 242.4 V	1.26% with output voltage 237 V
Equal carriers-PODPWM	2.31% with output voltage 242.7 V	2.21% with output voltage 242.8 V	2.23% with output voltage 241.5 V	2.17% with output voltage 243.1 V	1.89% with output voltage 240.2 V	2.15% with output voltage 243.4 V	2.17% with output voltage 243.9 V	1.30% with output voltage 237 V
Equal carriers-APODPWM	2.13% with output voltage 242.9 V	2.11% with output voltage 242.8 V	2.07% with output voltage 243.5 V	2.07% with output voltage 243.5 V	1.93% with output voltage 240.3 V	2.01% with output voltage 244.4 V	2.33% with output voltage 243.5 V	1.21% with output voltage 236.9 V
Equal carriers-COPWM	1.91% with output voltage 247.6 V	2.25% with output voltage 248.8 V	2.58% with output voltage 249.5 V	2.54% with output voltage 248.8 V	1.70% with output voltage 246.2 V	2.74% with output voltage 249.4 V	2.33% with output voltage 247.6 V	1.02% with output voltage 239.7 V

Table 8
THD% For Unequal Amplitude of Carriers Different Modulation Strategies After Filtering Across Various Frequencies.

Modulation strategies	THD% 2 kHz	THD% 3.5 kHz	THD% 4 kHz	THD% 4.5 kHz	THD% 5 kHz	THD% 5.5 kHz	THD% 8 kHz	THD% 10 kHz
Un-Equal carriers-PDPWM	3.24% with output voltage 246.2 V	1.28% with output voltage 248.3 V	0.43% with output voltage 247.9 V	0.53% with output voltage 248.6 V	0.30% with output voltage 246.3 V	0.97% with output voltage 249 V	1.83% with output voltage 246.2 V	1.10% with output voltage 242 V
Un-Equal carriers-PODPWM	0.50% with output voltage 244.8 V	0.24% with output voltage 249.5 V	0.46% with output voltage 250.2 V	0.31% with output voltage 249.4 V	0.41% with output voltage 246.6 V	0.31% with output voltage 248.5 V	0.31% with output voltage 247.6 V	1.09% with output voltage 241.8 V
Un-Equal carriers-APODPWM	1.08% with output voltage 179.1 V	2.10% with output voltage 180.2 V	3.49% with output voltage 180 V	2.74% with output voltage 180.7 V	4.00% with output voltage 178 V	3.12% with output voltage 180.6 V	3.98% with output voltage 179 V	4.73% with output voltage 176.2 V
Un-Equal carriers-COPWM	2.63% with output voltage 244.9 V	2.97% with output voltage 245.1 V	2.94% with output voltage 244.4 V	3.17% with output voltage 245.3 V	2.46% with output voltage 242.5 V	3.17% with output voltage 245.5 V	2.68% with output voltage 244.9 V	1.89% with output voltage 237 V

Table 9
THD% For Unequal Amplitude of Carriers POD-PWM Strategy Across 3.5 kHz Frequency.

Modulation strategy	Resistive load 50Ω	Resistive load 500Ω	Resistive load 1kΩ	Resistive load 1.5kΩ	Resistive load 2kΩ
UEAPOD-3.5 kHz PWM	0.12%	0.14%	0.17%	0.20%	0.24%

industrial inverters, is the carrier-based sinusoidal-pulse width modulation (S-PWM), given the fact that it is simple and capable of minimizing the THD of the output voltage [22-24]. The Multi-carrier level-shifted PWM (LS-PWM) strategies applied on the proposed Thirteen-level MPUC inverter using Matlab/Simulink are illustrated in Fig. 6. Fig. 6(a) represents the equal amplitude PD-PWM (EAPD-PWM), Fig. 6(b) the equal amplitude POD-PWM (EAPOD-PWM) strategy. Fig. 6 (c) equal amplitude APOD-PWM (EAAPOD-PWM), Fig. 6(d) equal amplitude CO-PWM (EACO-PWM), Fig. 6(e). unequal amplitude PD-PWM (UEAPD-PWM), Fig. 6(f). unequal amplitude POD-PWM (UEAPOD-PWM), Fig. 6(g) unequal amplitude APOD-PWM (UEAAPOD-PWM), and Fig. 6(h) unequal amplitude CO-PWM (UEACO-PWM) strategies. The sample carriers arrangement of the twelve triangular carrier signals (carriers; i= 1, 2, 3 … 12), the frequency of carriers is equal to 2 kHz and are disposed of vertically or overlapped to make the LS-PWM strategies with equal and unequal amplitudes regulate the sinusoidal reference signal of the same amplitude of peak-to-peak amplitude of carriers and frequency 50 Hz and use an amplitude modulation index (ma) equal to 1, and a frequency modulation index (mf) equal to = 40.

Comparing the sinusoidal signal to each carrier yields one if the sinusoidal is higher than the carrier signal and zero when the carrier is greater than the sinusoidal. The product of the comparison is employed to produce the gate-pulses that are correlated to the ON-OFF states, as illustrated in Table 3. As stated earlier, to generate zero-level, the control circuitry chooses either states 7 or 7', depending on the constant state of the IGBTs and the positivity/negativity of the reference waveform to reduce the switching frequency. On the one hand, the zero-level is generated at the output depending on state 7 if the reference signal is positive; when a negative value is attributed to the reference signal, the control circuit is caused to select state 7' to generate the zero-level.

MATLAB/Simulink is utilized to simulate the Thirteen-level MPUC to demonstrate its role in obtaining AC power from DC sources. The proposed inverter employs three DC voltage sources: V_1, V_2, and V_3, which have 100 V, 50 V, and 25 V, respectively. Fig. 7 displays The output waveform of Thirteen-MPUC without using PWM techniques is pointed out in Fig. 7(a) thirteen voltage levels over time, measured in seconds, with a peak voltage of 175 V. Fig. 7(b) then shows the output waveform after applying a low-pass LCL filter, tailored to our data's noise profile, to reduce high-frequency noise. The corresponding THD percentage of the topology without PWM presented in Fig. 7(c) is 26.25%, and 9.91% after applying the filter, as shown in Fig. 7(d) is estimated by adopting the FFT tool, which provides built-in functions for resampling, filtering, and outlier detection. To ensure accurate frequency domain analysis using MATLAB/Simulink, preprocess data by resampling, filtering, and removing outliers. Configure the solver parameters to use a fixed-step and Ode8 and set the Powergui Block settings to Discrete with a 50×10^{-6} sample time for achieving even sampling. Finally, visually and statistically inspect the processed data to confirm effective noise and outlier reduction.

To examine LS-PWM strategies implemented on Thirteen-MPUC with different frequencies, Table 4 provides the other simulation parameters employed to simulate LS-PWM strategies implemented on Thirteen-MPUC by using an amplitude modulation index equal to 1. Table 5 focuses on the THD values at various frequencies (2 kHz, 3.5 kHz, 4 kHz,

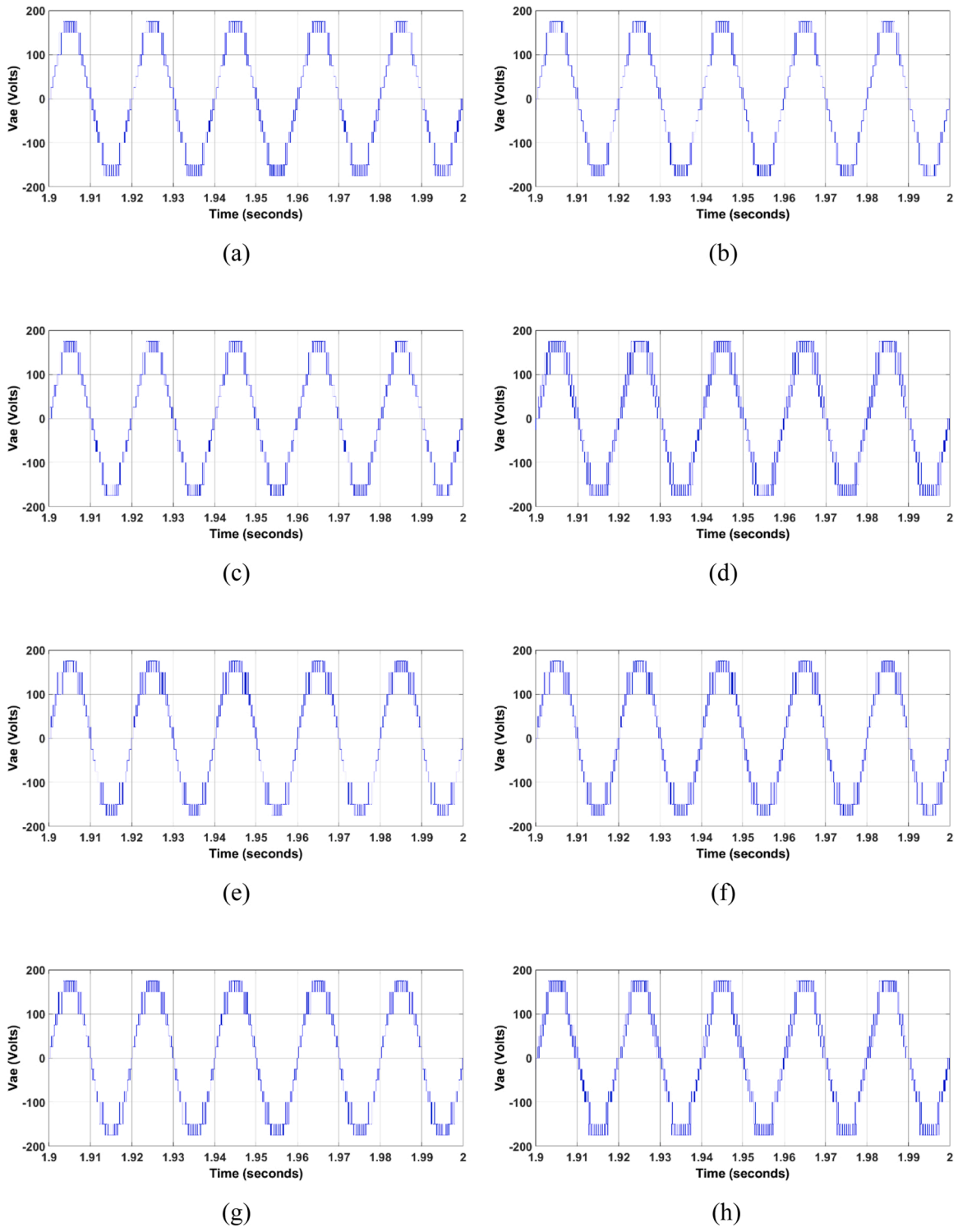


Fig. 8. The output voltage waveform of (a) EAPD-PWM, (b) EAPOD-PWM, (c) EAAPOD-PWM, (d) EACO-PWM, (e) UEAPD-PWM, (f) UEAPOD-PWM, (g) UEAAPOD-PWM, and (h) UEACO-PWM techniques before applying filter to the proposed inverter with a switching frequency equal to 2 kHz.

4.5 kHz, 5 kHz, 5.5 kHz, 8 kHz, and 10 kHz) along with the associated higher fundamental output voltage in volts for the proposed 13- levels MPUC inverter with sinusoidal reference to resistive load at the output, when applying equal amplitude of carriers for PD-PWM, POD-PWM, APOD-PWM, and CO-PWM methods before filtering.

Table 5 analysis reveals that the APODPWM and PODPWM methods effectively maintain lower THD levels across various frequencies. For equal carriers Among these, APODPWM demonstrates marginally superior performance in terms of both THD and output voltage stability. Conversely, despite yielding higher output voltages, the Carrier Overlapping PWM (COPWM) method leads to significantly greater THD levels. This outcome suggests a trade-off between achieving higher output voltage and minimizing harmonic distortion in these modulation strategies. Additionally, Table 6 shows the THD values at various frequencies with the associated higher fundamental output voltage in volts for the proposed 13- levels of MPUC inverter with sinusoidal reference to

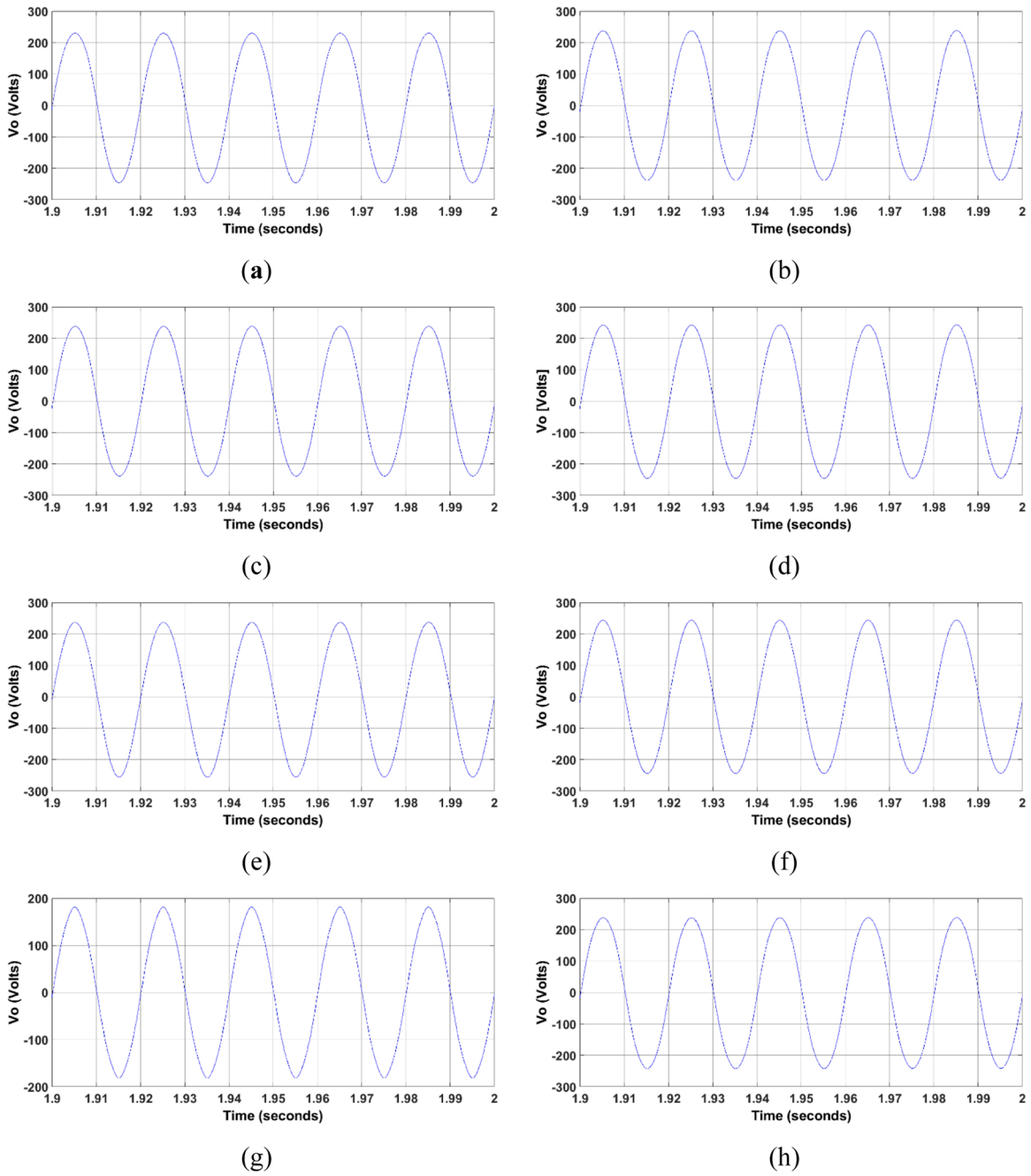


Fig. 9. The output voltage waveform of (a) EAPD-PWM, (b) EAPOD-PWM, (c) EAAPOD-PWM, (d) EACO-PWM, (e) UEAPD-PWM, (f) UEAPOD-PWM, (g) UEAAPOD-PWM, and (h) UEACO-PWM techniques applied on 13- level MPUC at a ON-OFF frequency equal to 2 kHz after applying filter.

resistive load at the output when applying unequal amplitude of carriers for PD-PWM, POD-PWM, APOD-PWM, and CO-PWM methods before filtering.

The unequal amplitude of carriers-PDPWM (UEAPD-PWM) and Un-Equal carriers-PODPWM (UEAPOD-PWM) show relatively lower THD values across most frequencies compared to the other two strategies, suggesting better performance in terms of harmonic distortion. The output voltage tends to decrease with increasing frequency. Still, UEAPOD-PWM and Unequal amplitude of carriers-APODPWM (UEAA-POD-PWM) tend to maintain a relatively stable output voltage across different frequencies compared to the others, and at higher frequencies (8 K and 10 K), there is a noticeable increase in THD for all strategies. Still, the growth is most pronounced in the Unequal amplitude of carriers-COPWM (UEACO-PWM) strategy.

An LCL low-pass filter (LCL-LPF), commonly utilized in power electronics and specifically designed for stepped sine wave generation, comprises two inductors (L) and one capacitor (C) in a specific configuration. This type of filter aims to smooth out signals by attenuating high-frequency components above their cutoff frequency. In our application, where the generation involves 26 steps within one 50 Hz cycle, the frequency of these steps is calculated as $f_{steps} = 50\ Hz \times 26 = 1300\ Hz$. Accordingly, we set the filter's cutoff frequency at 1/10th of this stepping frequency, equating to 130 Hz. This configuration effectively eliminates higher frequency components that may arise during the stepping process of a 50 Hz waveform, thereby minimizing interference with the desired signal.

When applied to a step waveform, the LCL-LPF significantly influences its characteristics, notably its peak voltage. The filter's step

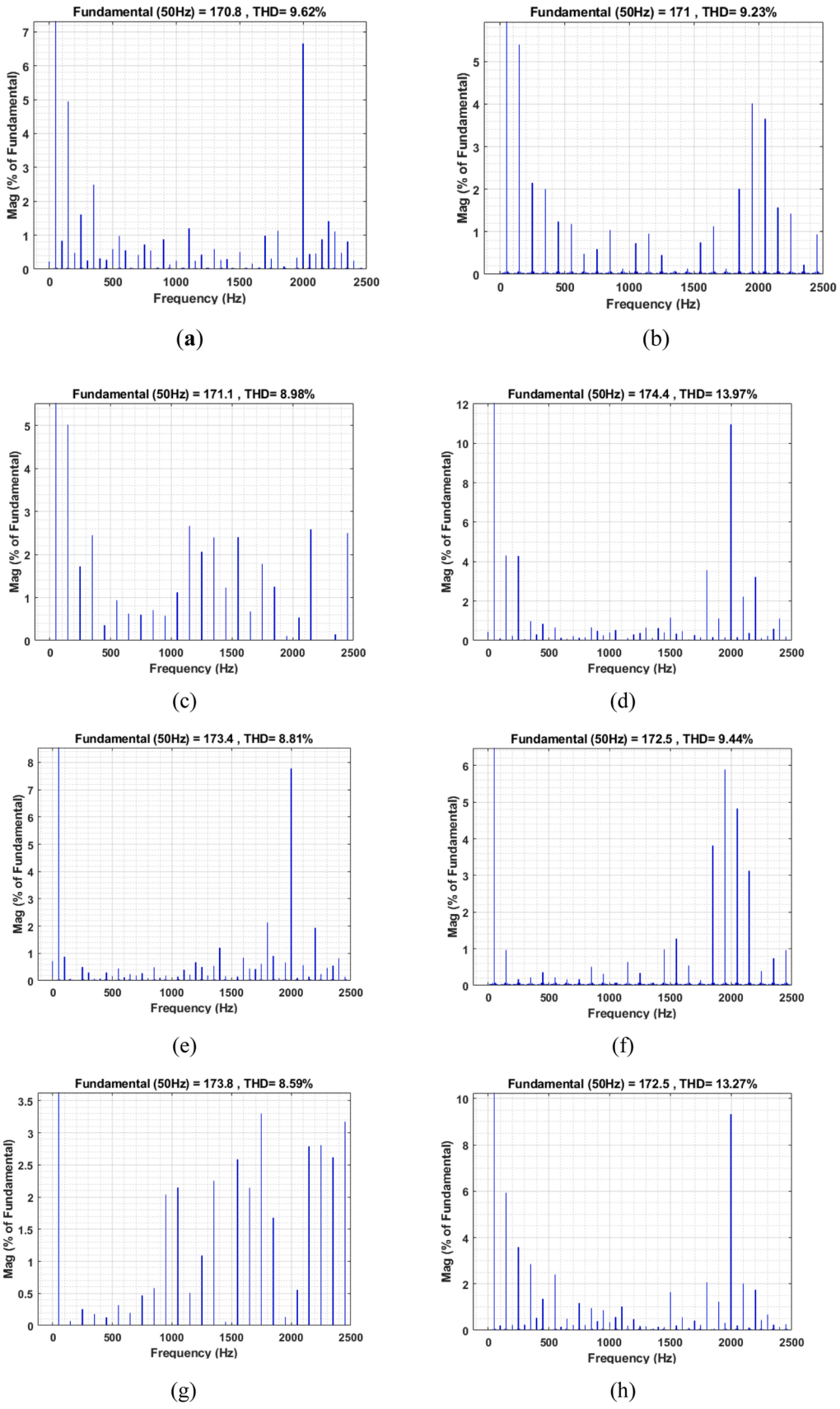


Fig. 10. FFT analyzer of the output voltage waveform of (a) EAPD-PWM, (b) EAPOD-PWM, (c) EAAPOD-PWM, (d) EACO-PWM, (e) UEAPD-PWM, (f) UEAPOD-PWM, (g) UEAAPOD-PWM, and (h) UEACO-PWM techniques applied on Thirteen- level MPUC at a ON-OFF frequency equal to 2 kHz before applying filter.

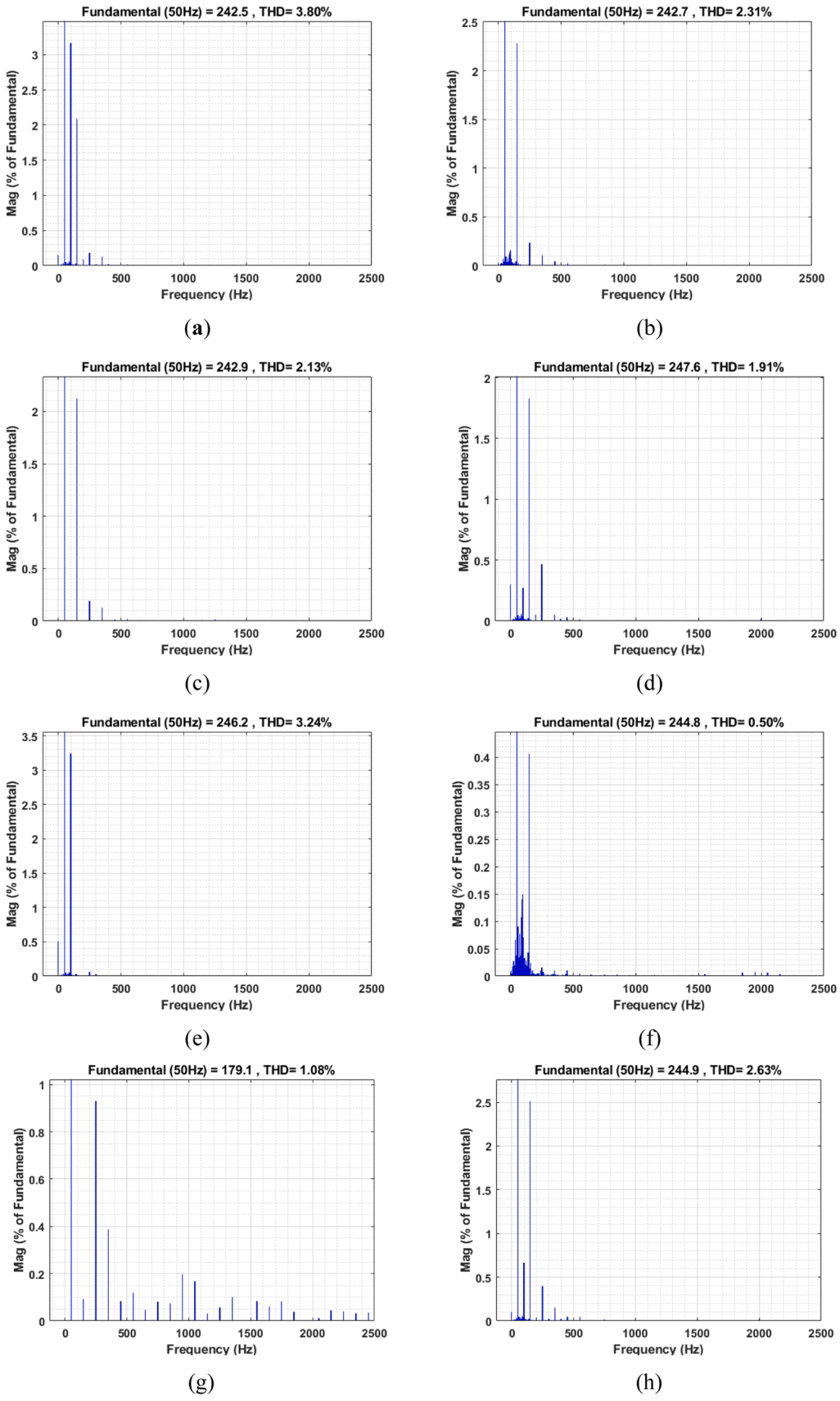


Fig. 11. FFT analyzer of the output voltage waveform of (a) EAPD-PWM, (b) EAPOD-PWM, (c) EAAPOD-PWM, (d) EACO-PWM, (e) UEAPD-PWM, (f) UEAPOD-PWM, (g) UEAAPOD-PWM, and (h) UEACO-PWM techniques applied on Thirteen- level MPUC at a ON-OFF frequency equal to 2 kHz after applying filter.

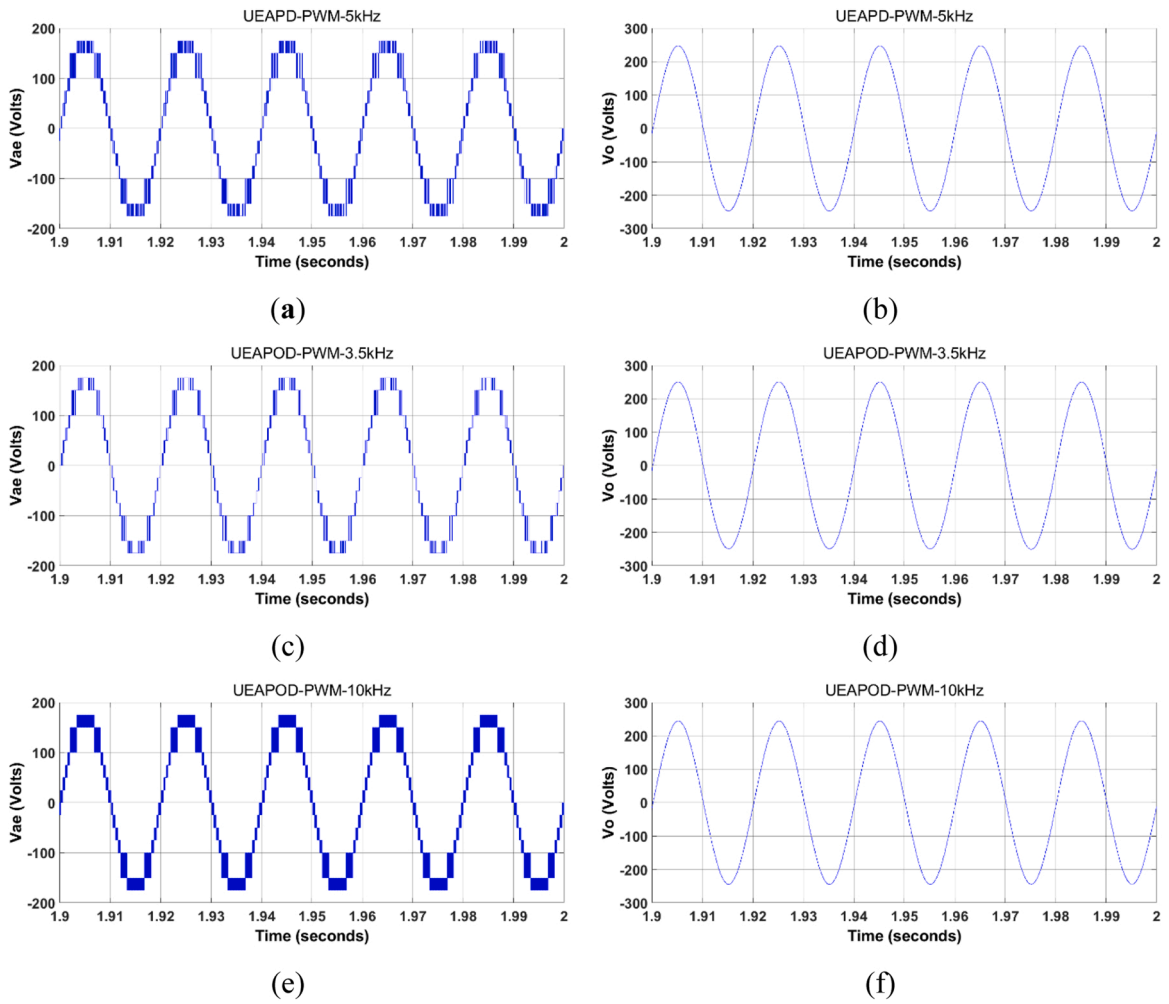


Fig. 12. (a) The output voltage waveform before the filter of the UEAPD-PWM strategy was applied on Thirteen-level MPUC at the ON-OFF frequency of 5 kHz. (b) The output voltage waveform after the filter of the UEAPD-PWM strategy was applied on Thirteen-level MPUC at the ON-OFF frequency of 5 kHz. (c) The output voltage waveform before the filter of the UEAPOD-PWM strategy was applied on Thirteen-level MPUC at the ON-OFF frequency of 3.5 kHz. (d) The output voltage waveform after the filter of the UAPOD-PWM strategy was applied on Thirteen-level MPUC at the ON-OFF frequency of 3.5 kHz. (e) The output voltage waveform before the filter of the UEAPOD-PWM strategy was applied on Thirteen-level MPUC at the ON-OFF frequency of 10 kHz. (f) The output voltage waveform after the filter of the UEAPOD-PWM strategy was applied on Thirteen-level MPUC at the ON-OFF frequency of 10 kHz.

response typically includes an initial peak surpassing the steady-state value, indicative of its transient response and not an increase in the original waveform's peak. Furthermore, the filter's response to the step input often encompasses a temporary phase with oscillatory behavior attributable to resonance between the inductors and the capacitor. This phase may exhibit overshot, where the peak voltage temporarily exceeds the original level. However, this overshoot is transient and does not suggest a permanent LCL-LPF. It is intricately designed to smooth out waveforms, with its impact on peak voltage contingent on the filter's unique characteristics and the properties of the step waveform. Typically seen in LCL filter designs, the transient response may result in temporary voltage overshoots. However, it's crucial to note that this filter does not permanently elevate the peak voltage of the original waveform in its steady state. Instead, it's adeptly engineered to eliminate undesirable high-frequency components, particularly in our application involving a stepped sine wave.

When conducting 13-level MPUC topology across various switching frequency ranges with an LCL filter, it is imperative to fine-tune the filter in alignment with the altered stepping frequency. Any changes in the number of steps or the base frequency (originally set at 50 Hz) necessitate recalculating the stepping frequency. Table 7 shows the THD values at various frequencies with the associated higher fundamental output voltage in volts for the proposed 13- levels of MPUC inverter with sinusoidal reference to resistive load at the output when applying equal amplitude of carriers for PD-PWM, POD-PWM, APOD-PWM, and CO-PWM methods, as well as Table 8 shows the THD values when using unequal amplitude of carriers for PD-PWM, POD-PWM, APOD-PWM, and CO-PWM methods after filtering.

The equal amplitude of carriers-COPWM generally shows the lowest THD values across most frequencies after using the filter, with a notable lowest THD at 10 K frequency, indicating high effectiveness in reducing harmonic distortion. Equal amplitude of carriers-APODPWM and Equal amplitude of carriers-PODPWM also demonstrate low THD values but slightly higher than COPWM, suggesting good performance in minimizing harmonic distortion. For applications requiring the lowest possible THD, and higher output voltage is preferred, the Equal amplitude of carriers-COPWM strategy seems to be the best option, especially at higher frequencies. The other strategies (PDPWM, PODPWM, and APODPWM) balance THD performance and output voltage stability, making them suitable for applications where moderate THD levels are acceptable. UEAPD-PWM and UEAPOD-PWM, particularly in the Un-Equal amplitude of carrier's category, show superior performance in low THD and high output voltage.

With a 13-level MPUC topology incorporating a missing level in the

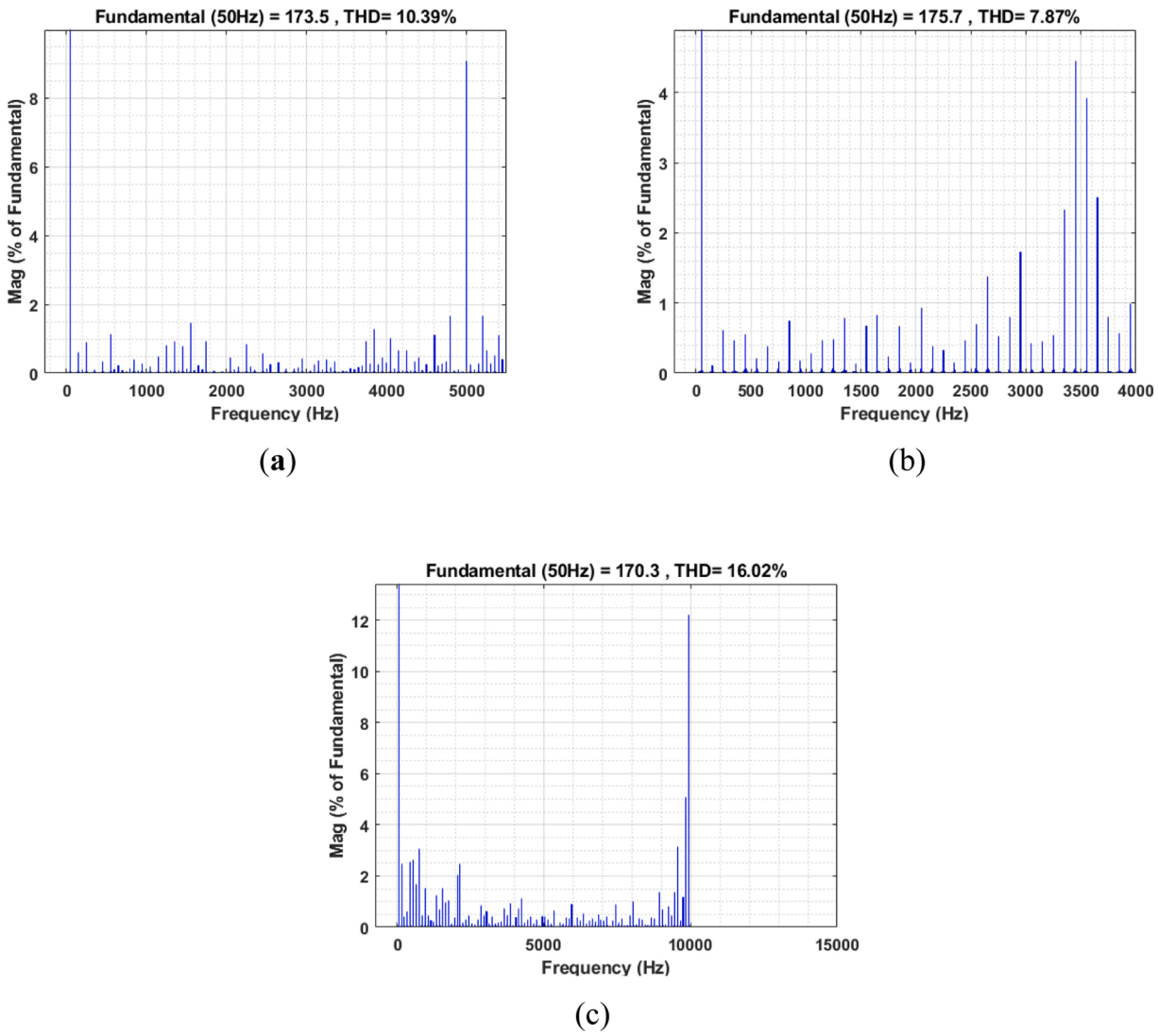


Fig. 13. Total harmonic distortion of the produced voltage of (a) UEAPD-PWM with a switching frequency equal to 5 kHz, (b) UEAPOD-PWM with a switching frequency equal to 3.5 kHz, and (c) UEAPOD-PWM with a switching frequency equal to 10 kHz strategies applied on Thirteen- level MPUC before applying the filter.

stepped wave, we can discern the effectiveness of Equal and Unequal amplitude of carrier modulation strategies in terms of THD and output voltage at various frequencies.

THD Performance:

- Unequal amplitude of Carriers: These strategies typically show lower THD values across the frequency spectrum, which is crucial for a 13-level MPUC topology with a missing level. UEAPD-PWM and UEAPOD-PWM demonstrate remarkably low THD, making them highly suitable for applications sensitive to harmonic distortion.
- Equal amplitude of Carriers: While THD values for Equal amplitude of carriers are relatively higher, they still perform well. EACO-PWM stands out with the lowest THD among Equal amplitude carriers.

Output Voltage Stability:

- Unequal amplitude of Carriers: These strategies exhibit high and stable output voltages, suitable for applications requiring consistent voltage levels. UEAPD-PWM and UEAPOD-PWM maintain voltages consistently above 240 V.
- Equal Carriers amplitude: Also displays stable and high output voltage, especially notable in EACO-PWM.

Effectiveness in 13-Level MPUC Topology:

- The Unequal amplitude of carrier strategies are more adept at compensating for the missing level in a stepped wave, indicating a better fit for the complexities of a 13-level MPUC topology.
- Equal amplitude of carriers, while effective, might not be as optimized for this specific topology as the Unequal amplitude of carriers.

This analysis plays a vital role in evaluating the performance of the proposed thirteen-level MPUC inverter topology across diverse load conditions. As evidenced in Table 9, the impact of varying resistive loads on the UEAPOD-PWM is notably minimal. This outcome suggests that the proposed inverter topology retains its efficiency consistently, even when employing different level-shifted multi-carrier PWM (LS-PWM) topologies at various frequencies.

Now, Fig. 8 represents the output voltage waveform of (a) EAPD-PWM, (b) EAPOD-PWM, (c) EAAPOD-PWM, (d) EACO-PWM, (e) UEAPD-PWM, (f) UEAPOD-PWM, (g) UEAAPOD-PWM, and (h) UEACO-PWM techniques before applying filter to the proposed inverter. These techniques are applied to the proposed inverter with a switching frequency equal to 2 kHz. It presents the output voltage, which can reach an ultimate voltage of about 175 V, the sum of the three DC sources. The 13-level MPUC inverter at the ON-OFF frequency of 2 kHz generates

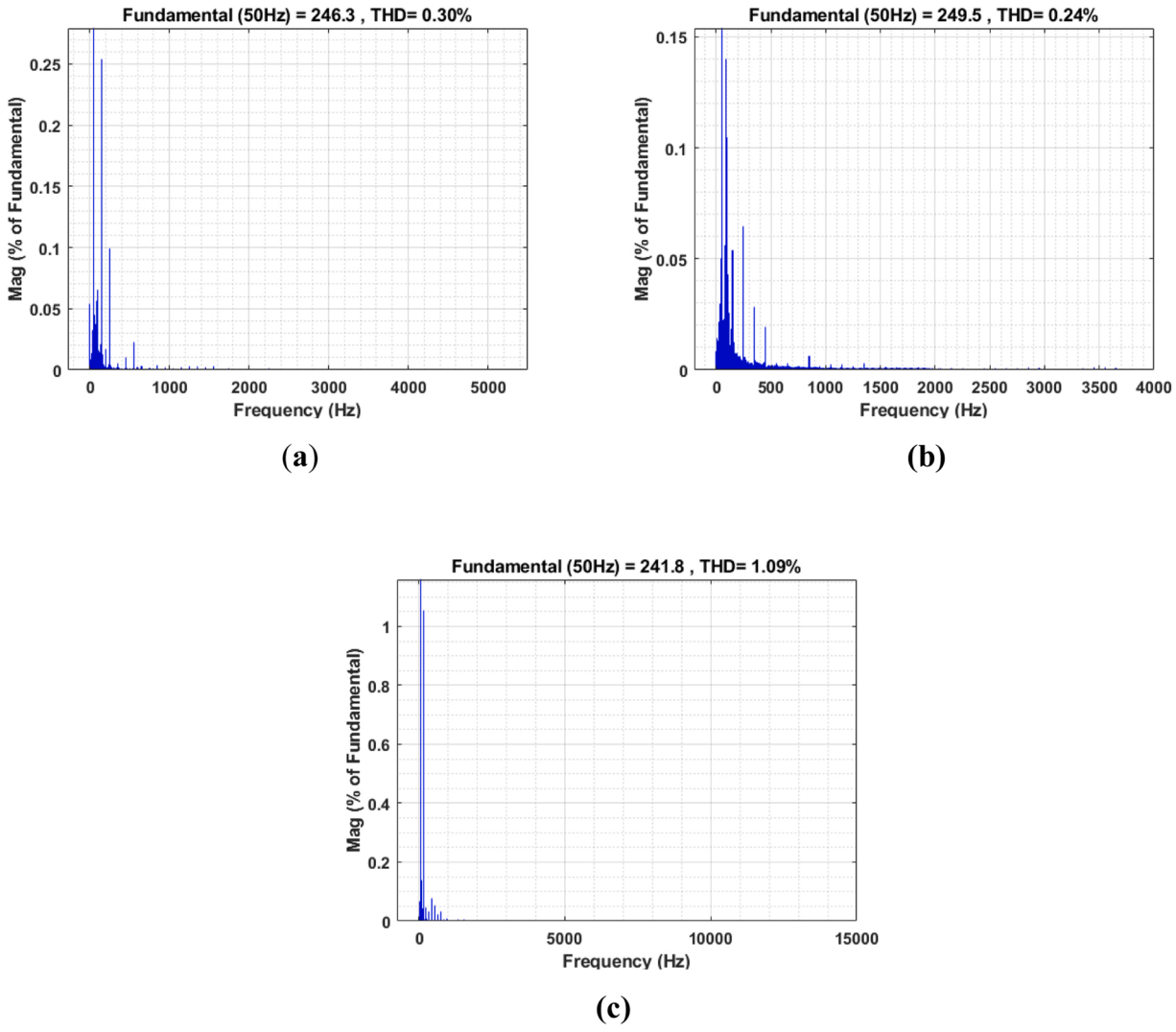


Fig. 14. Total harmonic distortion of the produced voltage of (a) UEAPD-PWM with a switching frequency equal to 5 kHz, (b) UEAPOD-PWM with a switching frequency equal to 3.5 kHz, and (c) UEAPOD-PWM with a switching frequency equal to 10 kHz strategies applied on Thirteen- level MPUC after applying the filter.

Table 10
Experimental Components for 13-Level MPUC.

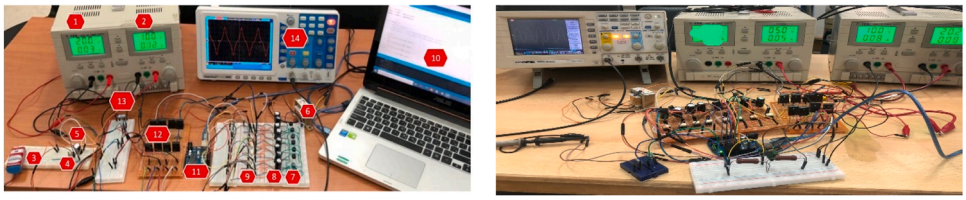
#	THD
1,2	A dual power supply as DC-sources V_1, V_2
3,4,5	Voltage regulator as DC-source V3
6	Transformer 220/12volt 1 A
7	Eight Bridge Rectifiers 2 A
8	Eight Capacitors 1000 u 35 V
9	Eight of TLP250's Isolated IGBT Drive [31]
10	Switching Code using a microcontroller
11	Microcontroller
12	Eight, HGTG30N60C3D IGBTs [32]
13	Resistive load (1kΩ)
14	Inductive RL-Load (1kΩ) (10 mH)
15	Digital Oscilloscope

smooth waveforms after applying the LCL filter, as pictured in Fig. 9. The spectrum analyzer is conducted on the output voltage waveform, as represented in Fig. 10, without any harmonics filter. Also, the spectrum analyzer is performed on the output voltage waveform, as illustrated in Fig. 11. In comparison, it uses a harmonics LCL filter.

Next, Fig. 9 displays the output voltage waveform of (a) EAPD-PWM, (b) EAPOD-PWM, (c) EAAPOD-PWM, (d) EACO-PWM, (e) UEAPD-PWM, (f) UEAPOD-PWM, (g) UEAAPOD-PWM, and (h) UEACO-PWM techniques after applying filter to the proposed inverter. These techniques are applied to the proposed inverter with an ON-OFF frequency of 2 kHz. It presents the output voltage, which can reach a smooth waveform voltage of about 240 V due to applying the LCL filter. The output voltage waveform is analyzed using a spectrum analyzer at an ON-OFF frequency of 2 kHz before and after applying the LCL filter presented in Figs. 10 and 11.

UEAPOD-PWM shows exceptionally low THD values across all frequencies, with the highest being only 1.09% at the ON-OFF 10 kHz frequency, indicating its high effectiveness in minimizing harmonic distortion. For applications requiring the lowest THD and low ON-OFF frequency, Unequal carriers-PDPWM and Un-Equal carriers-PODPWM would be preferable due to their lower THD values and higher voltage levels. Unequal carriers-PDPWM perform well with THD values, particularly the harmonic distortion factor of the output voltage, which is 0.30%. The amplitude of the carrier is evident at the ON-OFF frequency of 5 kHz, and for Unequal carriers-PODPWM, the harmonic distortion factor of the output voltage is 0.24%. The amplitude of the carrier is evident at the ON-OFF frequency of 3.5 kHz.

Furthermore, Fig. 12 displays the produced voltage waveforms of the UEAPD-PWM technique with a switching frequency equal to 5 kHz, the UEAPOD-PWM technique with a switching frequency equal to 3.5 kHz, and the UEAPOD-PWM technique with a switching frequency equal to



(a) (b)

Fig. 15. Experimental setup pictorial view of Thirteen- level MPUC (a)Using resistive load, (b)Using inductive load.

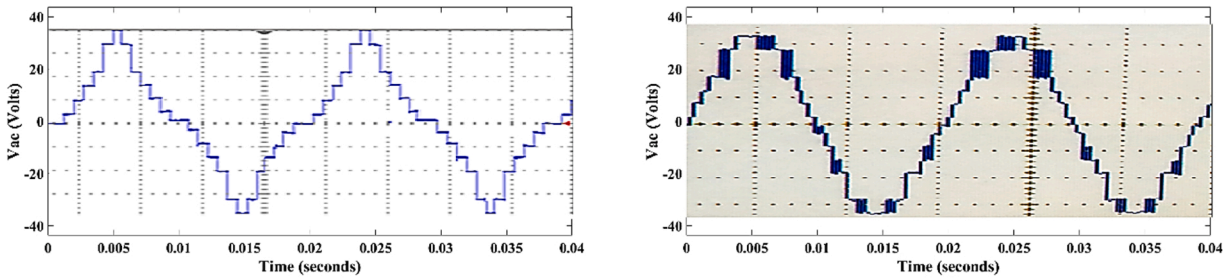


Fig. 16. The experimental output voltage of the proposed Thirteen- level MPUC while using resistive load (a) without PWM strategy. (b) with UEAPD-PWM strategy.

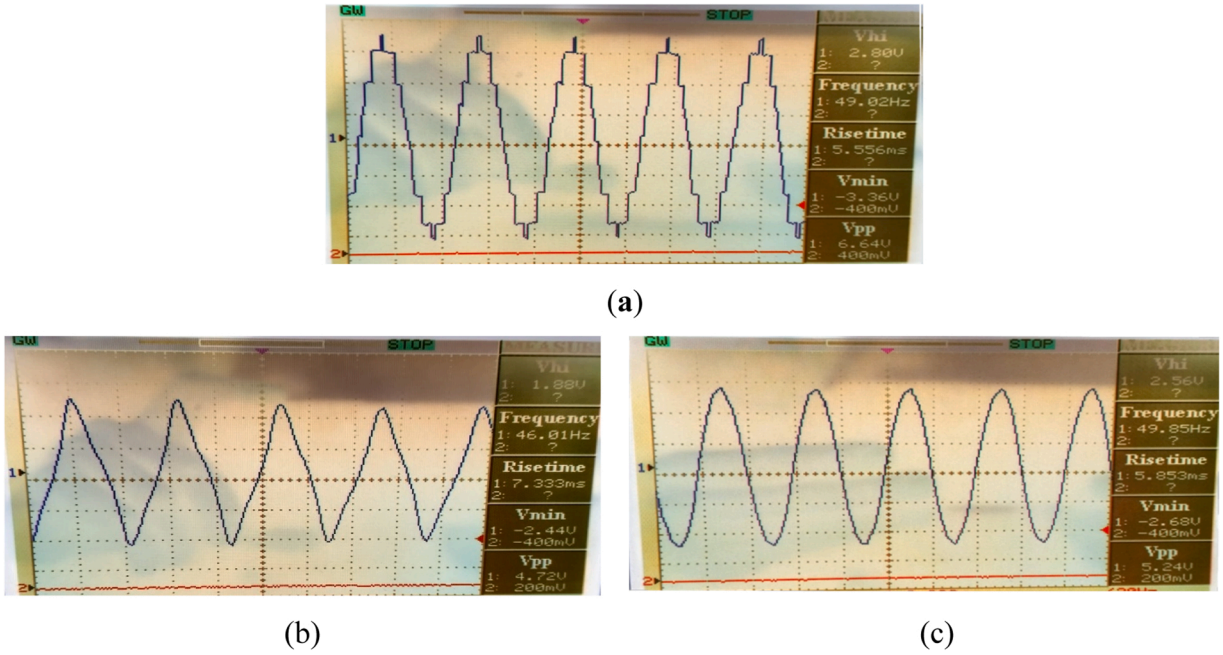


Fig. 17. The experimental output voltage of the proposed Thirteen-level MPUC while using inductive load(a) without the filter. (b) with 1st order filter. (c) with 2nd order filter.

10 kHz techniques applied to the proposed inverter.

Fig. 12 displays the output voltage waveform before and after applying the filter on the proposed topology of (a) Unequal carriers-PDPWM at ON-OFF 5 kHz frequency, (b) Un-Equal carriers-PODPWM at ON-OFF 3.5 kHz frequency, EAPOD-PWM at ON-OFF 10 kHz frequency.

Moreover, Fig. 13 demonstrates the harmonic spectra of the output voltage of the UEAPD-PWM technique with a switching frequency equal to 5 kHz, UEAPOD-PWM technique with a switching frequency equal to 3.5 kHz, and UEAPOD-PWM technique with a switching frequency equal to 10 kHz, all of which were applied to the proposed inverter, resulting in THD values of 10.39% %, 7.87%, and 16.02% respectively, the THD values before using the filter.

To comply with the IEEE519 standard [20] and generate a THD $\leq$ 5% waveform while suppressing the unwanted harmonics, an LCL filter has been implemented between the inverter and the load, reducing the voltage and current harmonics absorbed by the proposed inverter. Fig. 12 illustrates the smoother voltage output waveforms after filtration. Additionally, Fig. 14 demonstrates the harmonic spectra of the output voltage of the UEAPD-PWM technique with a 5 kHz switching frequency, the UEAPOD-PWM technique with a 3.5 kHz switching frequency, and the UEAPOD-PWM technique with a 10 kHz switching

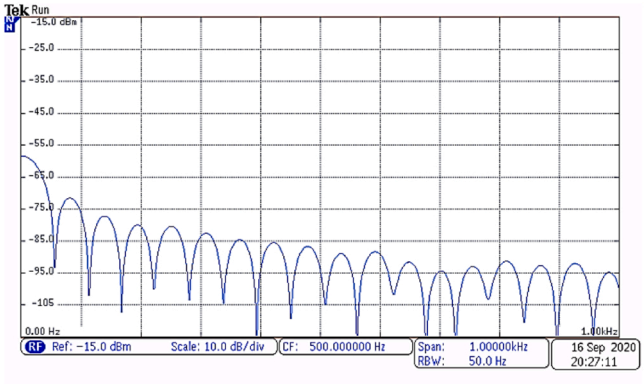


Fig. 18. The experimental spectrum of the output voltage of the proposed Thirteen-level MPUC.

Table 11
Comparison Between Proposed Topology and Other topologies.

	NPC	FC	CHB	PUC	MPUC	13-MPUC
REF.	[6]	[29]	[6, 25]	[13]	[19]	[21] our work
O/P Voltage Levels	13	13	13	7	7	13
Clamping Diodes	22	0–4	0	0	0	0
Flying Capacitors	0	4	0	0	0	0
DC-Links Capacitors	12	0	0	1	0	0
Main Switches	24	13–18	24	6	6	8
DC-Sources	1	2	6	1	2	3

frequency. When applied to the proposed inverter, these techniques resulted in harmonic distortions of 0.30%, 0.24%, and 1.09%, respectively.

3.2. Experimental results

Eight IGBT switches (600 V, 30 A, HGTG30N60C3D) were used in the current study to build the 13-MPUC inverter. A gate-driver circuit is used to produce the switching signals of the IGBTs [25,26]. Control of the eight switches and generation of PWM signals are executed through a switching algorithm implemented on Microcontrollers ATmega328p and ATmega2560. The ATmega328p is implemented to obtain the output voltage without any modulation technique, while the ATmega2560 is used to investigate the effect of the PWM modulation technique in real-time controllers [27]. All the devices that were used in the experimental studies for Resistive load and Inductive load (RL load) are presented in Table 10 and have been outlined in Fig. 15(a) and Fig. 15(b). To emulate the solar system's power operation, three independent DC sources (V_1, V_2, and V_3) have been linked to the 13-MPUC as DC-power lines. Table IV shows all experimental test parameters.

In real-time implementation, three DC sources are used: the first VDC is 20 V, the second VDC produces 10 V, and the third VDC is 5 V. Consequently, the peak output voltage of the 13-MPUC topology with a resistive load of 1 kΩ, becomes 35 V with a frequency of 50 Hz. Fig. 16 (a) demonstrates the result of the output voltage waveform of the 13-MPUC without the application of PWM techniques.

It is worth noting that the voltage output amplitude is approximately 35 V, with the digital oscilloscope volt/div equals 1 V, and attenuator-probe (X10 probe) is used. As depicted in Fig. 16(a), the 13-level voltage is generated to create the output waveform of the 13-MPUC topology because of the regulation of DC voltages at desirable references, where V_2 is equal to half of V_1 and V_3 equals half of V_2. Moreover, the 13-MPUC inverter works very well with the UEAPD-PWM strategy. It generates the output waveform as represented in Fig. 16(b) due to the regulation of DC voltages at the desired references, where V_1 equals 20 V, V2 equals 10 V, and V3 equals 5 V. The peak-to-peak output voltage of the 13-MPUC topology with an inductive RL-load becomes 66.4 V with a frequency of 49.02 Hz, as shown in Fig. 17(a). The resulting output voltage waveform of 13-MPUC with a 1st-order low pass RC filter is 47.2 V with a frequency of 46.01 Hz, as demonstrated in Fig. 17(b). In Fig. 17(c), the output voltage waveform of 13-MPUC with a 2nd-order low pass RC filter reaches 52.4 V with a frequency of 49.85 Hz. Finally, Fig. 18 illustrates the experimental spectrum of the output voltage generated by the proposed 13-level MPUC. This measurement was conducted under a resistive load condition without PWM techniques.Top of Form

4. Discussion

To effectively demonstrate the effectiveness of our proposed topology, we conducted a comparison with conventional MLI topologies such as NPC, FC, and CHB, as well as some recently developed reduced-switch topologies like PUC and MPUC [6,13,19,28–30]. Implementing MLIs typically incurs high costs due to the large number of semiconductor switches involved. Table 11 illustrates the significance of our proposed topology in terms of component count and level generation compared to other topologies. It's worth noting that, except for the PUC topology, all mentioned MLI topologies can generate 13 levels of voltage [6], Our 13-MPUC topology, as detailed in reference [21], advances the multi-level inverter design. A notable breakthrough is the production of a reference sine wave, vital for applications like PV modules and DC sources. This is achieved by employing three separate DC sources, a typical approach for such configurations. The magnitude of this sine wave is the sum of the voltages from these DC sources, which operate at a 50 Hz frequency. This aspect is crucial for the inverter's operation. Our design addresses both cost-efficiency and performance improvement. Additionally, it showcases reduced total harmonic distortion due to fewer conducting switches needed for each level of generation, as demonstrated in Table 11. This represents a significant advantage over conventional topologies.

5. Conclusions

This paper addresses the design and implementation of a 13-level MPUC inverter. The proposed inverter in the current study utilizes three DC sources and eight switches. It is effectively controlled using triangular wave-Multicarrier LS-PWM techniques at various frequencies to study the harmonics. Various types of level shifted multicarrier PWM were compared, and the harmonic distortion in the output voltage waveforms was investigated. Furthermore, an LCL-filter was integrated into the inverter's output, along with the various LS-PWM control strategy, to effectively suppress unwanted harmonics.

The results indicated that The harmonic distortion of Unequal Phase Opposition Disposition PWM (UEAPOD-PWM) shows exceptionally low THD values across high frequency exhibited a THD 1.09% at the ON-OFF 10 kHz frequency, For applications requiring the lowest THD and low ON-OFF frequency, Unequal Phase Opposition Disposition PWM (UEAPOD-PWM) had the lowest a THD of 0.24% at the ON-OFF frequency of 3.5 kHz, and Unequal carriers-PDPWM (UEAPD-PWM) would be preferable too due to their lower THD values and saturated higher voltage levels exhibited a THD of 0.30% at the ON-OFF frequency of 5 kHz. Furthermore, the proposed inverter achieves high-power quality, very low harmonic distortion for different resistive loads, and small filter size.

In the real-time implementation, the 13-MPUC inverter produces thirteen levels of voltage at a frequency of 50 Hz, both without the use of PWM techniques and when applying the UEAPD-PWM technique. Based on this study, the proposed thirteen levels modified packed U-Cells inverter achieves an efficient performance both in simulation and experimental results.

In summary, the benefits of the 13-MPUC inverter are notable. It

allows the use of three different photovoltaic panels with varying output voltage ratings, each linked to DC converters. The 13-MPUC inverter can combine the three DC voltages at its output, resulting in a 13-level voltage while maintaining a high-power factor when connected to the grid. The utilization of various range of switching frequencies, and a small number of IGBTs in the 13-MPUC configuration contributes to minimizing the THD content in the 13-level stepped wave voltage, thereby increasing the inverter's efficiency. However, it's important to note that the 13-MPUC is not currently connected to the grid. Therefore, for further validation of the proposed topology's performance, it can be applied in conjunction with various photovoltaic systems as DC power sources, enabling it to connect to the grid for enhanced utilization.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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