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ORIGINAL ARTICLE

Investigation of gate leakage current in TFET: A semi-numerical approach

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Abstract Tunneling FET (TFET) has been demonstrated as a favorable candidate to replace conventional MOSFETs in low-power applications. However, there are many challenges that should be overcome to efficiently operate the TFET. One of the most limiting factors that can restrict the TFET performance is the gate leakage current. In this paper, the tunneling leakage current through the gate oxide of double gate TFET has been analyzed. The conduction band energy level for gate-oxide-silicon was employed to calculate the tunneling transmission coefficient by utilizing a numerical method. To obtain the potential barrier between the gate and the channel surface, a modified analytical pseudo-2D method has been applied to deduce the corresponding surface potential taking into account a precise calculation of depletion regions. Furthermore, the inclusion of the image charge barrier lowering effect is incorporated in calculating the transmission probability through the oxide. Including such an effect shows a significant influence on determining the gate tunneling current. The gate leakage current has been calculated for various bias voltages and equivalent oxide thicknesses. The presented semi-numerical technique shows good agreement within a suitable CPU time when validated and compared against full numerical TCAD simulation.

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1. Introduction

Scaling down the device dimensions aims to accomplish higher chip density, better speed, and lower power consumption [1]. In addition, the scaling of the voltage supply leads to a quadratic reduction of the dynamic power consumption. To achieve the same ON-state current, the threshold voltage has to be proportionally scaled while reducing the supply voltage. These modifications cause an exponential rise of the OFF-state leakage current (I_{OFF}) in Metal Oxide Semiconductor FET (MOSFET) as its feature size decreased down to the nanometre dimension. Further, the current switching process in MOSFET occurs due to the thermionic injection of charge carriers over an energy barrier; consequently, the subthreshold swing (SS) is thermally limited to a value of 60 mV/dec [2]. These two constraints along with other short channel effects (SCEs) may restrict the future usability of MOSFET, especially in low-power applications.

To overcome the MOSFET limitations, alternative new devices like Tunnel FET (TFET) are being investigated [3,4]. TFET devices use quantum mechanical band-to-band tunneling (BTBT) mechanism to inject carriers, rather than the thermal injection encountered in the conventional MOSFET. The subthreshold swing (S) can be expressed by [5],

$$S = \left(\frac{1}{V_{eff}}\frac{dV_{eff}}{dV_{GS}} + \frac{\xi + b}{\xi^2}\frac{\xi}{dV_{GS}}\right)^2 \ln(10) \quad (1)$$

where V_{eff} and ξ are the bias and the electric field at the tunnel junction, respectively, and $b = \frac{4\sqrt{m^*}E_g^{\frac{3}{2}}}{3q\hbar}$ where q is the electron charge, m^* is the effective mass, $\hbar$ is the reduced Planck's constant and E_g is the energy gap. The terms of Eqn. (1) are not explicitly limited by the thermal voltage. This could cause the subthreshold slope to be smaller than 60 mV/dec, at 300 K. Further, the device tunneling mechanism makes the TFET almost insensitive and nearly independent of changes in temperature. Therefore, TFETs can keep their excellent switching characteristics even at high temperatures. Many research efforts have been performed to improve the performance of the TFET device operation. These include, for instance, proposing gate over source-channel overlap pockets [6], vertical gate-based elevated tunnel source [7], drain-engineering quadruple-gate design [8], line-TFET utilizing dual MOS-capacitor extensions [9], incorporating low band gap in the source like semiconducting silicide and Germanium [10,11], increasing the gate-source overlap [12], using hetero gate dielectric [13], and many other techniques [14,15].

Although exhibiting better I_{ON}/I_{OFF} switching and a lower I_{OFF} mainly governed by the p-i-n reverse diode, the gate leakage current caused by the very thin gate oxides remains an important issue that limits the performance of the device and increases power consumption [16]. The tunneling of the charge carriers across the gate oxide caused by the high electric field resulting from scaling was thoroughly studied in the last decades for MOSFETs [17,18]. However, its influence on TFET performance has not been well investigated in the literature. The ON-state current in TFETs is directly affected by the BTBT path of the electrons through the barrier width. Decreasing the gate oxide thickness causes a narrower tunneling width between the source and the channel interface owing to the strong control of the gate voltage, which in turn improves the tunneling probability and ameliorates I_{ON} [19]. However, when reducing the gate oxide thickness, the gate leakage current cannot be neglected. Therefore, tunneling through the gate is a critical parameter that must be included in TFET analysis. Few studies, for instance, high k-dielectrics [20], gate stacks [21], and recently, non-uniform gate oxide thickness [22] have been published to investigate the gate leakage in TFETs and possible ways to alleviate its influence on the device performance. Thus, more efforts are needed to explore the influence of gate leakage current in order to be able to implement such an effect into circuit simulators to predict TFET circuits performance and their reliability. In this work, we report on a semi-numerical approach to model TFETs, including gate leakage current, as a first try to achieve a physically based model which can be extended to be implemented for circuit applications.

Notably, the leakage can occur between the gate and the channel but also between the source or drain overlap region and the gate. This paper deals with a structure geometry that does not involve overlapping. From the potential barrier aspect, tunneling is divided into either direct tunneling or Fowler-Nordheim tunneling. To be able to derive the tunneling current, two main quantities are essential: the supply function and the transmission probability. The transmission probability should be attained by solving Schrodinger's equation. But due to the complexity of obtaining an analytical solution for some potential functions, several approximation methods were developed. WKB [23] and Gundlach methods [24] are the most commonly used techniques. However, one of the restrictions of both methods is that they are only applied to linear potential barriers. Further, the reduction in size for double gate devices imposes the inclusion of the image force effect, as mentioned in [25], altering the potential in a non-linear shape. Its influence on the current magnitude is clearly demonstrated. Therefore, numerical methods akin to the transfer-matrix approach are successfully used to obtain an exact solution for gate current for a single dielectric gate oxide of different thicknesses. In our analysis, we utilize an analytical solution for the surface potential to get the barrier along the oxide semiconductor interface. Then, we employ Transmission Line Method (TLM) numerical technique [26] to compute the gate tunneling current.

The remainder of the paper is planned as follows. The DG-TFET structure along with its key parameters is introduced in Section 2. An analytical solution is presented in Section 3.1 to deduce the surface potential for the device and consequently to obtain the oxide barrier potential which is a trapezoidal-like shape. To calculate the transmission probability, the TLM numerical technique is introduced. The approach used for the current calculation is explained in Section 3.2. Finally, the potential influenced by the image force as well as the transmission probability and deducted currents are compared with the results of the 2-D device simulator ATLAS from Silvaco in Section 4. The paper is summarized, and conclusions are provided in the last section.

2. Device structure and main simulation parameters

A lateral Double Gate n-type TFET structure is illustrated in Fig. 1(a). The drain current results from the carriers tunneling from the source valence band to the lightly doped channel

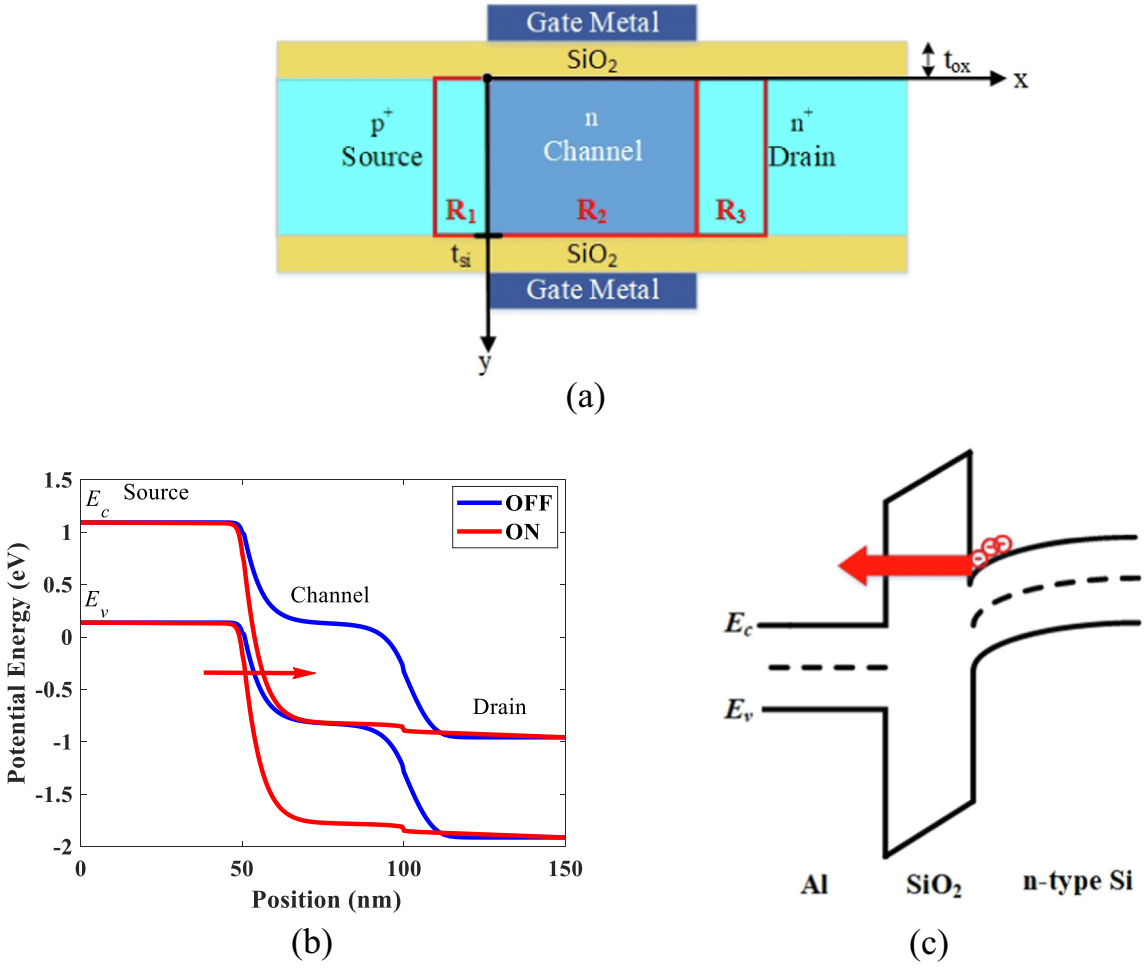

Fig. 1 (a) Main DG-TFET structure showing different basic regions (b) energy band diagram for ON and OFF TFET state conditions (c) schematic energy band diagram through of Al-SiO_2-nSi.

conduction band as illustrated in Fig. 1(b) for both ON and OFF states. These carriers are then carried to the drain region by the drift–diffusion process. The gate leakage current, which is the subject of our analysis, is caused by the electron tunneling through the gate dielectric, specifically silicon dioxide (SiO_2), or any other dielectric material, as represented in Fig. 1(c). The x-axis is specified along the length of the device while the y-axis, pointing positively downward, represents the thickness of the silicon body. To be able to analytically model our device to get the surface potential, three regions were defined: R_1 is the source depletion region; R_2 corresponds to the lightly doped channel region; and finally, R_3 is the drain depletion region as demonstrated in Fig. 1(a). Table 1 lists the main device parameters, including doping and geometrical dimensions. In addition, the work function (φ_m) of the gate metal electrode is taken as 4.3 eV. It should be pointed out here that the main factor that describes the oxide effect is the equivalent oxide thickness (EOT) which is defined as the thickness of SiO_2 (whose dielectric constant κ is 3.9) which would be required to accomplish similar capacitance density as any other high-κ oxide material used. For instance, an EOT of 1 nm can be obtained when an HfO_2 (whose κ = 16) layer, has a physical thickness of about 4 nm. So, the following analysis can be applied to any high-κ oxide materials that have the same EOT.

Table 1 Device Structure Parameters.

Parameter	Value
Source doping (/cm^3)	1×10^{20}
Channel doping (/cm^3)	1×10^{15}
Drain doping (/cm^3)	5×10^{18}
Source Length (nm)	50
Channel Length (nm)	50
Drain Length (nm)	50
Body Thickness (nm)	10
Gate EOT (nm)	1
ϵ_{rox}	3.9

3. Formulation of analytical and numerical techniques

3.1. Surface potential modelling

The potential barrier across the oxide was deduced by calculating the surface potential across the channel. Among the methods [27–30] existing to acquire the surface potential analytically in a TFET, the most used one is the pseudo 2D approach. Pseudo 2D method was originally developed for MOSFET [31]. Generally, analytical solutions involve simplifications on a mathematical model. In this regard, the pseudo 2D method aims to simplify the 2D Poisson's equation into a second-order 1D Poisson equation whose solution gives the surface potential. In [32], a pseudo-2D solution of Poisson's equation that includes the junction depletion regions inside the source and the drain in addition to the channel region was adapted for TFET devices. The approach provided in [30,32] is used in our analysis with a minor modification to get more accurate physically based calculations of depletion regions which, in turn, provides a precise representation of the surface potential.

The 2D Poisson's Equation, for a potential $\psi(x,y)$ is expressed as,

$$\frac{\partial^2\psi(x,y)}{\partial x^2}+\frac{\partial^2\psi(x,y)}{\partial y^2}=\frac{qN_j}{\varepsilon_{si}} \tag{2}$$

where N_j is the doping that corresponds to the region being analyzed and the subscript j corresponds to the region number (1 for R_1, 2 for R_2 and 3 for R_3). The continuity of the potential and the electric field at the vertical boundaries can be formulated as,

$$\begin{aligned}\psi(x,0)&=\psi_s(x)\\ \psi(x,t_{si})&=\psi_b(x)\end{aligned} \tag{3}$$

$$\begin{aligned}E_x(x,0)&=-\tfrac{\eta}{t_{si}}\left(V_{Geff}-\psi_s(x)\right)\\ E_x(x,t_{si})&=-\tfrac{\eta}{t_{si}}\left(\psi_s(x)-V_{Geff}\right)\end{aligned} \tag{4}$$

In these equations, $\psi_s(x)$ is the front-side (at $y=0$) surface potential (which is the same as rear-side (at $y=t_{si}$) surface potential). The effective gate potential, $V_{Geff}j$ for each region, is given by,

$$V_{Geff}j=V_G-V_{FBj} \tag{5}$$

where V_G is the gate bias w.r.t to the grounded source and V_{FBj} is the flat band potential which could be expressed as follows,

$$V_{FBj}=\phi_m-\chi-\frac{E_g}{2}+V_{bij} \tag{6}$$

Where the gate work function is denoted by ϕ_m, while the electron affinity is symbolized by χ and E_g is the energy band gap. The built-in potential, V_{bij} is given by,

$$V_{bij}=\begin{cases}V_T ln\left(\frac{N_1}{n_i}\right)\text{ for } j=1\\ V_T ln\left(\frac{N_2}{n_i}\right)\text{ for } j=2\\ -V_T ln\left(\frac{N_3}{n_i}\right)\text{ for } j=3\end{cases} \tag{7}$$

The parameter η in Equation (4) is defined as, $\eta=C_{oxj}/C_{Si}$ where C_{ox} is the oxide gate capacitance while C_{si} is the Si-film capacitance. These capacitance components could be given by,

$$C_{si}=\frac{\epsilon_{si}}{t_{si}} \tag{8}$$

$$C_{oxj}=\begin{cases}\frac{f_j}{\pi}\frac{\epsilon_{ox}}{t_{ox}}\text{ for } j=1 \text{ and } 3\\ \frac{\epsilon_{ox}}{t_{ox}}\text{ for } j=2\end{cases} \tag{9}$$

Unlike the conformal mapping technique [33] which is employed for regions R_1 and R_3, to consider the impact of the fringing field, we added a variable f_j which is taken as a fitting parameter to get the best fit for the depletion region versus TCAD simulation. It was found that this constant varies from 2 to 3 at the source region while its range is 0.1 to 0.3 at the drain region. It may be pointed out here that in the conformal mapping technique, the f_j value is taken to be fixed at 2 for both the source and the drain regions.

Now, after adopting the appropriate boundary conditions, one can find [34,35],

$$\psi_{sj}(x)=A_j e^{x/\lambda_j}+B_j e^{-x/\lambda_j}+\psi_{dj} \tag{10}$$

where, λ is the characteristic length and the potential ψ_d are given by,

$$\begin{aligned}\lambda_j&=\tfrac{t_{si}}{\sqrt{2\eta_j}}\\ \psi_{dj}&=V_{Geff}j-{\lambda_j}^2\tfrac{qN_j}{\epsilon_j}\end{aligned} \tag{11}$$

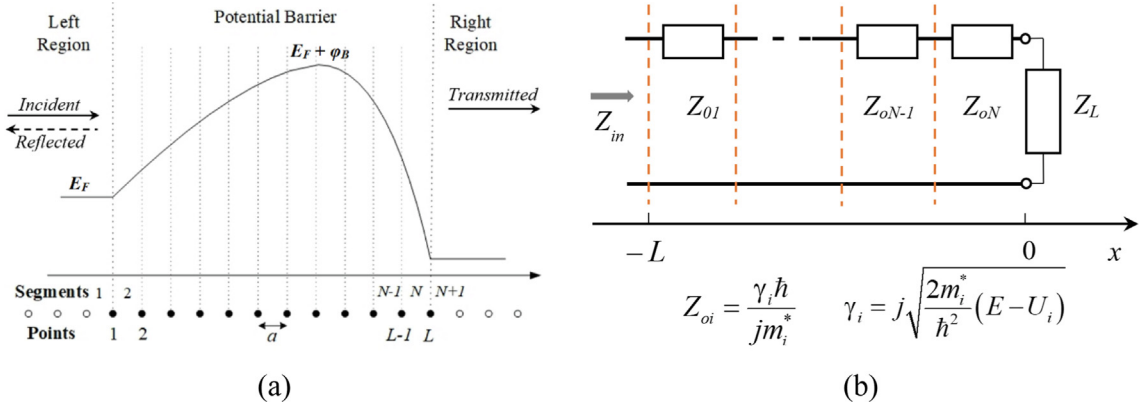

Fig. 2 (a) Energy band diagram for an arbitrary potential barrier showing the discritization criteria and (b) transmission line (terminated in an impedance Z_L) analogy.

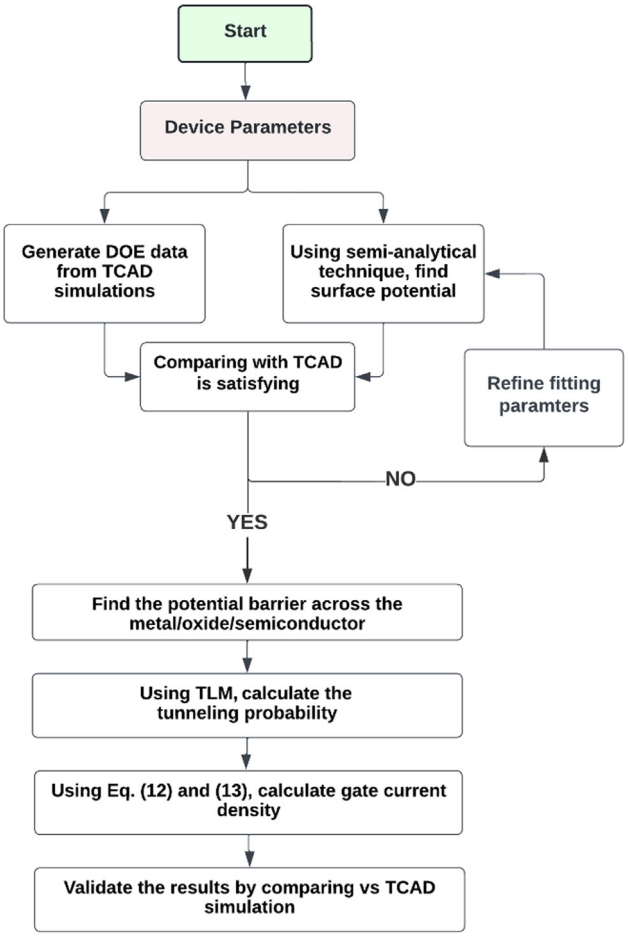

Fig. 3 A flowchart representing the steps carried out to perform the simulation of gate current through the oxide of a TFET structure.

Applying horizontal boundary conditions (continuity of surface potential and its derivative), the coefficients A_j and B_j can be deduced for the three regions. The depletion pn junction equations used in [32] are not used here. Instead, the equations are solved iteratively in order to get the depletion regions confirming zero field at the depletion edges as in [30].

3.2. Transmission probability and current calculation

To be able to calculate the transmission probability, the gate-oxide–semiconductor under study is segmented into M slices, each of those are divided into L points with uniform spacing a. The schematic band diagram of each slice can be illustrated as in Fig. 2(a). A space-discretizing method that is applied to the insulator, is the TLM which is considered a powerful and widely used technique [36,37]. There are also other numerical analysis techniques like transfer matrix method [38] and quantum transport model based on non-equilibrium Green's function (NEGF) [39,40]. In our analysis, the TLM is employed thanks to its easier implementation, higher convergence, and lower simulation time than the other candidates.

The TLM is used to evaluate the quantum mechanical wave impedance which enables for the transmission probability to be computed. In this technique, the barrier of an arbitrary potential is analogous to the junction between two distinct lossy transmission lines. In addition, the wavefunctions and their derivatives are comparable to the transmission line voltage and current, respectively. Fig. 2(b) illustrates the analogy of the lossy transmission line where each segment of the potential barrier is described by a portion of a transmission line whose characteristic impedance is Z_o that can be calculated based on the complex propagation constant γ and the effective mass m^*. The propagation constant depends on the difference between a given energy E and the potential (U) related to the barrier at the specified segment. The range of energies is taken to cover all values up to the barrier height. So, if the Fermi

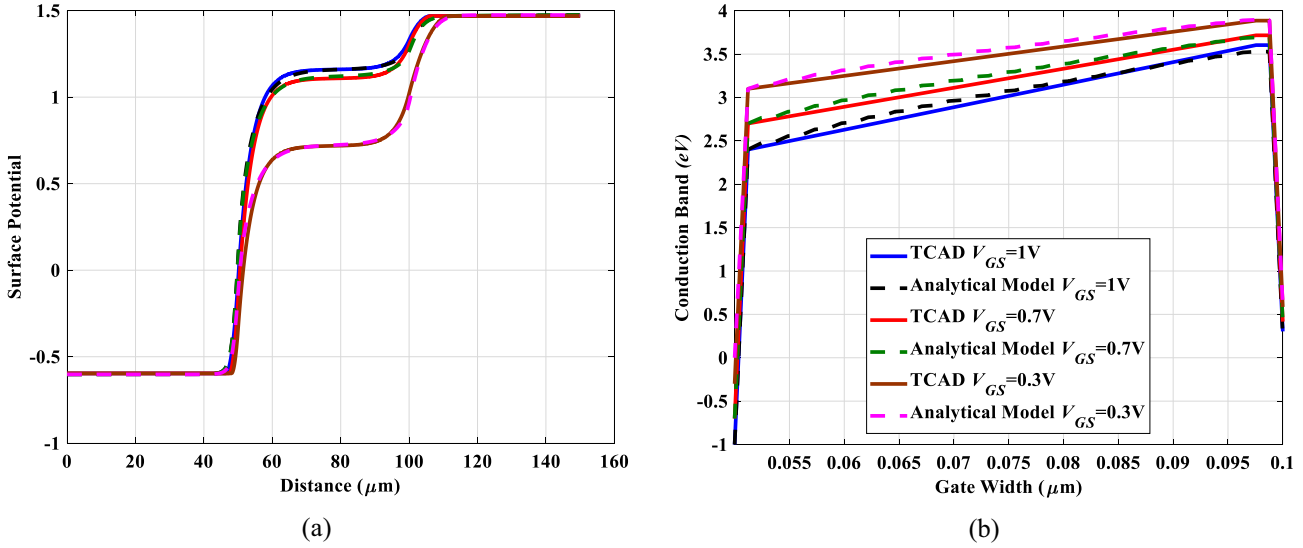

Fig. 4 Analytical model results vs TCAD simulation (a) surface potential ψ_S (V) vs. device length and (b) conduction band vs. gate oxide width at $M = 1$ for $V_{DS} = 1$ V and $V_{GS} = 1$, 0.7 and 0.3 V.

level at the left side of the barrier (see Fig. 2(a)) is E_F, then the energy range is $E_F < E < E_F + \varphi_B$, where φ_B is the barrier height as indicated in Fig. 2(a).

The approach to obtain the transmission probability using TLM is summarized as follows. Regarding the potential barrier displayed in Fig. 2(a), the values of γ and Z_o are first computed, for a certain energy E, employing constant values for m^* and V in each segment. The load Z_L ($=Z_{o,N+1}$) is represented by the characteristic impedance seen at segment $(N + 1)$. Next, when moving to sector $(N–1)$, the input impedance (Z_{N-1}) is evaluated by using the well-known transmission line input impedance equation taking the value of Z_L with $Z_o = Z_{o,N}$ and length a. Similarly, the input impedance Z_{N-2} is determined regarding Z_{N-1} as the load impedance. This repetitive procedure continues until we reach segment (1). Finally, the reflection coefficient for the given barrier is assessed using $Z_{o,1}$ as the characteristic impedance and Z_1 as the load impedance. A summary of the equations is given in Appendix A.

The gate oxide current density equation that models the direct tunneling process is commonly known as Tsu-Esaki equation [41] which is based on two main independent functions, the supply function $N(E)$ and the transmission coefficient $T(E, m_{ox})$. The current density is given as:

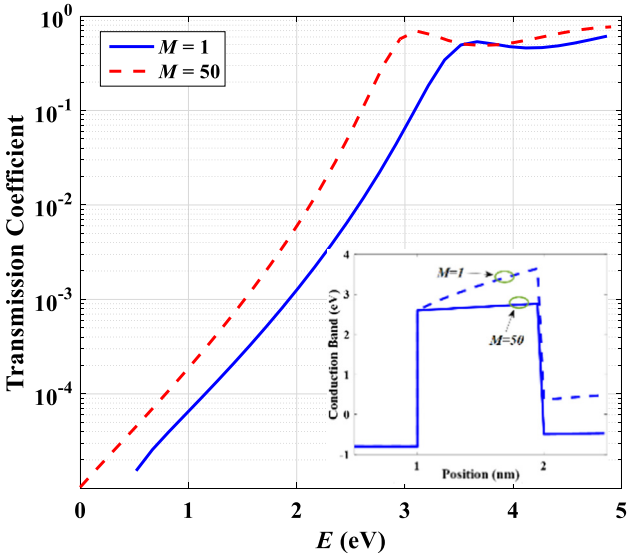

Fig. 6 Transmission coefficient at $V_{DS} = 0.5$ V and $V_{GS} = 0.8$ V for $M = 1$ and $M = 50$. The conduction band is illustrated in the inset of the figure.

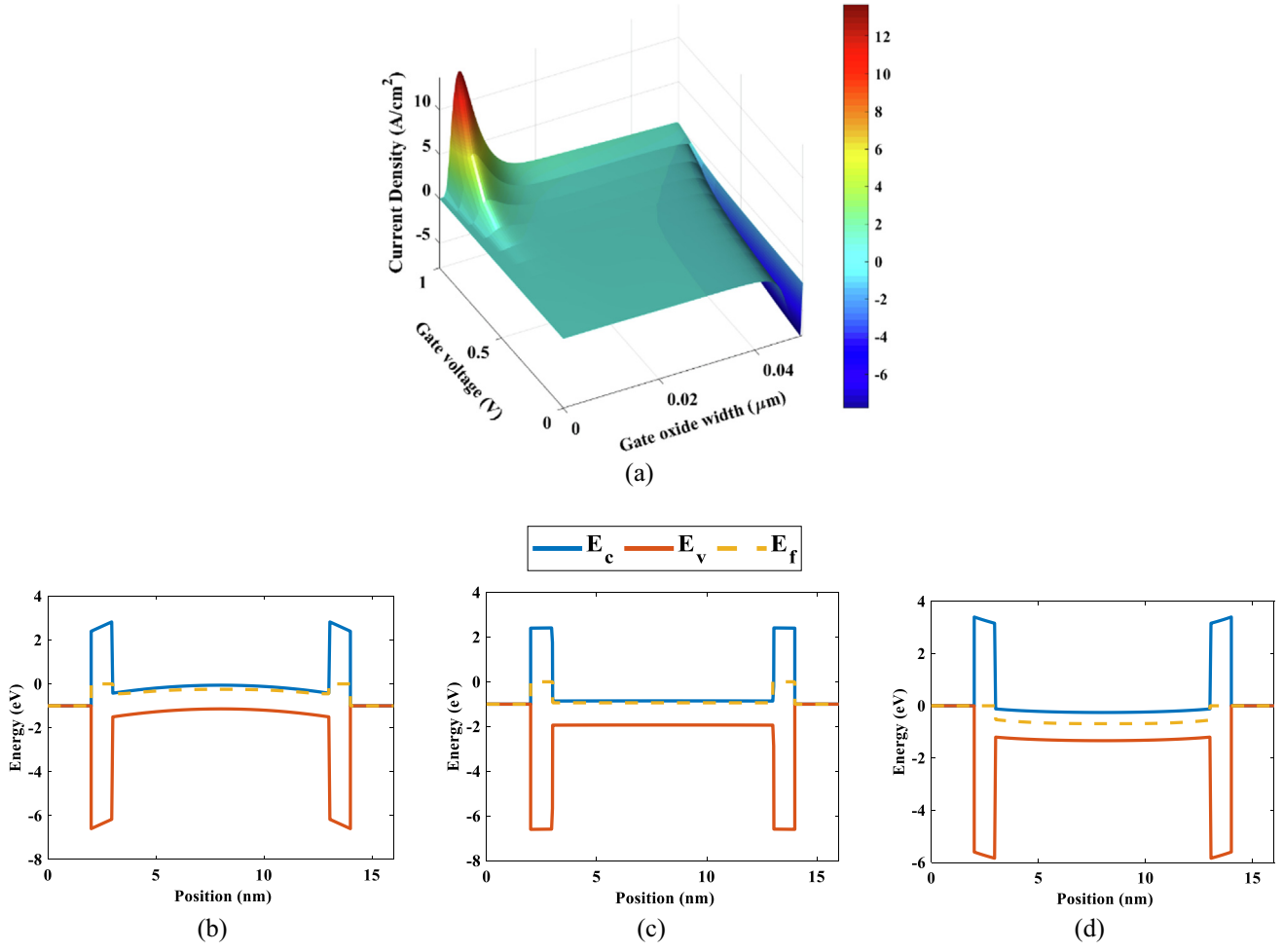

Fig. 5 (a) Current density surface plot at $V_{DS} = 1$ V and energy band diagram for $V_{DS} = 1$ V at (b) $V_{GS} = 1$ V at 0.004 μm (c) $V_{GS} = 1$ V at 0.045 μm (d) $V_{GS} = 0$ V at 0.045 μm.

$$J = \frac{4\pi m_{Si} q}{h^3} \int_{E_{min}}^{E_{max}} N(E) T(E, m_{ox}) dE \tag{12}$$

The supply function, assuming the Fermi-Dirac energy distribution, is given as:

$$N(E) = k_B T \ln\left(\frac{1 + exp\left(\frac{E_{fr} - E}{k_B T}\right)}{1 + exp\left(\frac{E_{fl} - E}{k_B T}\right)}\right) \tag{13}$$

where E_{fr} and E_{fl} are the quasi-Fermi level on both sides of the barrier.

As mentioned in [42], the electron DOS effective mass m_{Si} is deduced by a sum over the 6 valleys in the conduction band of silicon that yields to $m_{Si} = 2m_t + 4\sqrt{m_t m_l}$. The transverse effective mass, m_t, and the longitudinal mass, m_l, are set to 0.19 m_o and 0.92 m_o. The second electron mass m_{ox} used in the transmission coefficient is the dielectric electron mass. To obtain a reasonable resolution for the current density curve, 51 slices have been taken across the channel. The obtained conduction band in Section 3.1 is then used to get the transmission coefficient for the numerical method introduced. The effective mass of silicon dioxide,m_{ox}, is set to 0.77 m_o in accordance with the TCAD calibrated value [43].

A flowchart of the semi-numerical approach, utilized in this work, is displayed in Fig. 3. After inputting the device parameters and the physical models, we perform a design of experiments (DOEs) step to get required data from TCAD to be compared with the results obtained from the semi-numerical model of the surface potential. This step is carried out to confirm the validity of the presented model. Next, if the accuracy is accepted, the potential barrier across the metal/oxide/semiconductor is found. Then, by applying TLM, the tunneling probability is computed followed by calculating the gate current density using Equations (12) and (13). A validation step, by comparing the results of our technique vs those obtained from TCAD simulations, is performed in order to validate the proposed methodology.

4. Results & discussion

To validate our presented model results, TCAD simulations were accomplished in which the following models are applied.

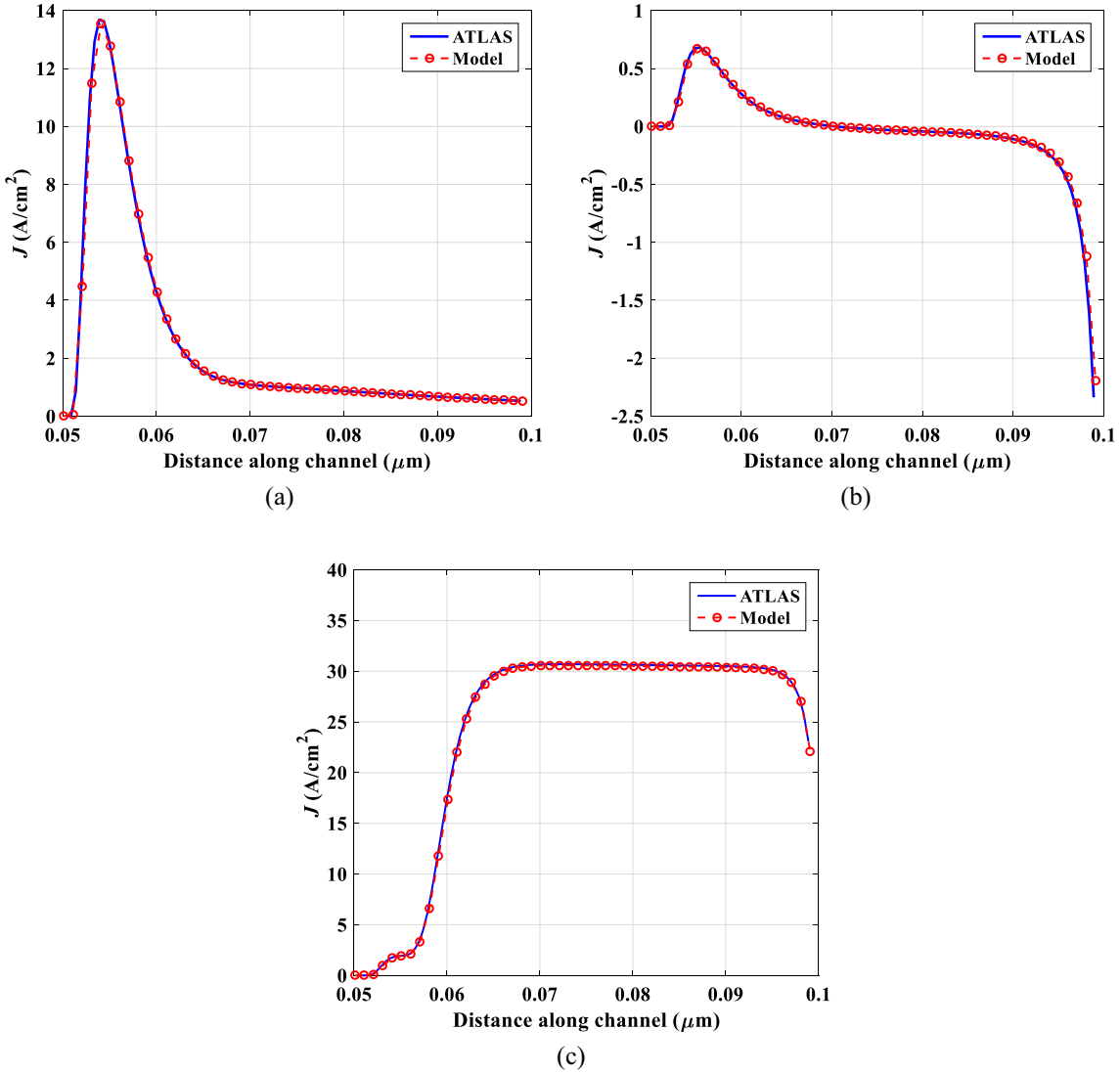

Fig. 7 Current density vs. distance along channel for: (a) V_{DS} = 1 V and V_{GS} = 1 V, (b) V_{DS} = 1 V and V_{GS} = 0.7 V and (c) V_{DS} = 0.5 V and V_{GS} = 0.8 V.

The self-consistent version of the Schenck oxide tunneling model is used. In this model, the effective mass is a significant factor that affects the tunneling current magnitude. Therefore, both electron and hole effective mass of SiO_2 are set to $0.77m_o$ according to [43]. To model the drain tunneling current, the non-local band to band tunneling model is adopted where the effective masses of both electron and holes are essential fitting parameters. To match with the results given in [44], the effective masses of both electron and holes are set to $0.1m_o$ and $0.17m_o$, respectively [45]. Field-dependence mobility is enabled to model any type of velocity saturation effect in silicon. Regarding carrier statistics, Fermi-Dirac statistics have been invoked.

To obtain a self-consistent evaluation of the leakage current in this work, the analytically obtained surface potential is initially plotted in Fig. 4(a) and compared vs TCAD simulations for V_{GS} equal and less than V_{DS}. Since surface potential correspondingly matches for different values of V_{GS}, the conduction band in the channel is deduced from the relation $E_c = -\psi_s + kT\ln\left(\frac{N_a}{n_i}\right)$. Consequently, the trapezoidal potential barrier through the oxide was easily constructed as displayed in Fig. 4(b).

To clarify the fluctuations of the gate leakage current density across the channel, a 3D-surface representation is shown in Fig. 5(a) for V_{DS} = 1 V and a gate voltage ranging from 0 to 1 V. For an applied gate voltage of 1 V, a positive current density appears at a distance of 0.004 μm away from the source-channel interface, as the result of the potential difference formed between the gate and the source as represented by the energy band diagram in Fig. 5(b). On the other extremity of the channel, there is no potential difference between the gate and drain clarified by the flattening of the conduction band in Fig. 5(c), resulting in a reduction of the leakage current. When the gate terminal is grounded, electrons are swept at the end of the channel toward the drain resulting in a negative current density flow justified by the negative band bending slope illustrated in Fig. 5(d).

Now, the TLM has been tested for a case study in which the applied voltages are V_{DS} = 0.5 V and V_{GS} = 0.8 V. The analysis starts by the calculation of the transmission coefficient $T(E, m_{ox})$, subsequently represented in Fig. 6 at the beginning of the channel (M = 1) and at the end of the channel (M = 50). The dependence of the transmission coefficient, for M = 50, on lower incident electron energy than for M = 1 is caused by the difference in both potential barrier heights as displayed in the inset of Fig. 6.

Next, the obtained $T(E, m_{ox})$ is substituted in Equation (12) to calculate the corresponding current density which is then compared with the one extracted from the simulator as shown in Fig. 7. At V_{DS} = 1 V and V_{GS} = 1 V, Fig. 7(a) shows a peak current at the beginning of the channel, due to the potential difference V_{GS} = 1 V, that gradually decreases, as previously explained in Fig. 5. As V_{GS} decreases, as in Fig. 7(b), the current at the beginning of the channel diminishes but a peak current at the end of the channel begins to appear. In Fig. 7(c), although the potential difference between the gate-source terminals is greater than the gate-drain terminals, a small current begins to appear at the beginning of the channel that largely increases as we move along the channel. The reason behind this is that the shape and magnitude of the current density across the channel are not only governed by the potential barrier bending due to the applied voltage over gate and drain electrodes, but also by the availability of carriers at the dielectric interface. This is clearly depicted in Fig. 8(a) by the energy band diagram at the left side of the channel that shows the separation between the Fermi level and the conduction band edge due to the proximity to the p-doped source, while at mid-point in the channel, shown in Fig. 8(b), the Fermi level and conduction band edge overlaps leading to a higher current. It is noted from the results that the TLM method exactly matches the simulator results.

It is worth mentioning that the TCAD simulator according to [46] uses a pseudo barrier method derived in [47] that enables the calculation of the transmission coefficient when

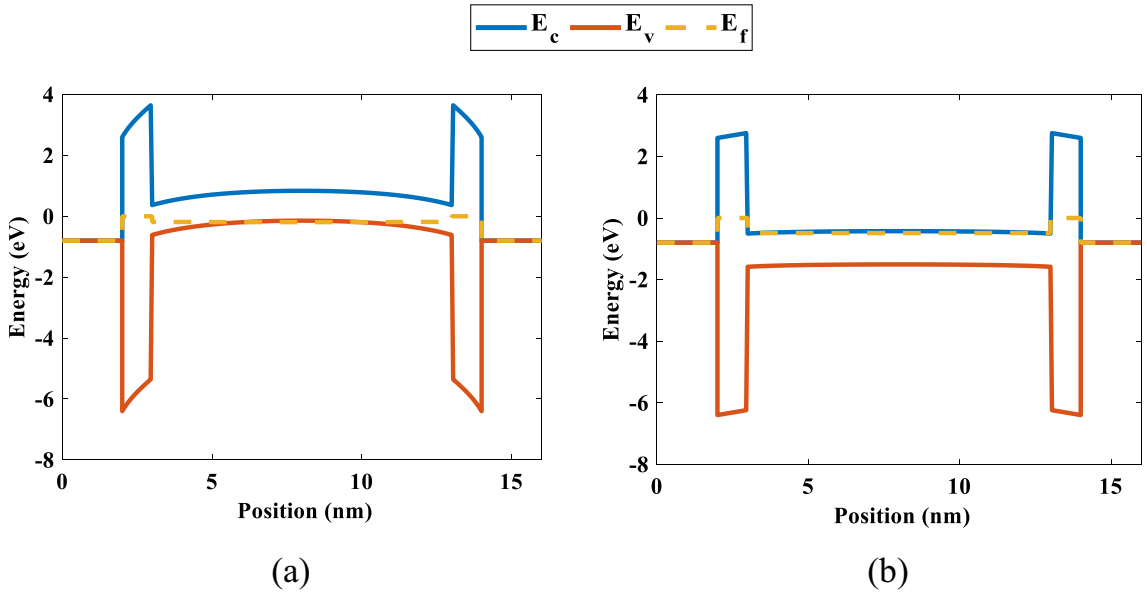

Fig. 8 Energy band diagram for V_{DS} = 0.5 V, V_{GS} = 0.8 V at a gate distance of (a) 0.05 μm (edge of source-channel interface) (b) 0.075 μm (mid-channel distance).

taking into consideration the image effect on a trapezoidal barrier. The influence of the image potential by both electrodes for a metal–insulator-semiconductor structure is derived in [48] as:

$$E_{im}(y_{ox}) = \frac{q^2}{16\pi\epsilon_{ox}} \times \sum_{n=0}^{\infty} (k_1 k_2)^n \left[\frac{k_1}{nd + y_{ox}} + \frac{k_2}{(n+1)d - y_{ox}} + \frac{2k_1 k_2}{(n+1)d}\right] \quad (14)$$

with $k_1 = \frac{\epsilon_{ox} - \epsilon_M}{\epsilon_{ox} + \epsilon_M} = -1$ and $k_2 = \frac{\epsilon_{ox} - \epsilon_{Si}}{\epsilon_{ox} + \epsilon_{Si}}$

The sum from 0 to 11 is found to be satisfying. Therefore, Equation (14) have been applied on all energy barriers. The build-up of this image charges lowers the barrier height and round-off its edges, and in consequence directly influences the transmission coefficient as depicted in Fig. 9, for $M = 25$ with $V_{DS} = 0.8$ V and $V_{GS} = 0.5$ V. Further, the magnitude of the current density is considerably affected as appears in Fig. 10 for the three investigated cases.

Finally, integrating the electron tunneling current density over the channel length enables the calculation of the total gate current. In Fig. 11, the gate current is illustrated for both

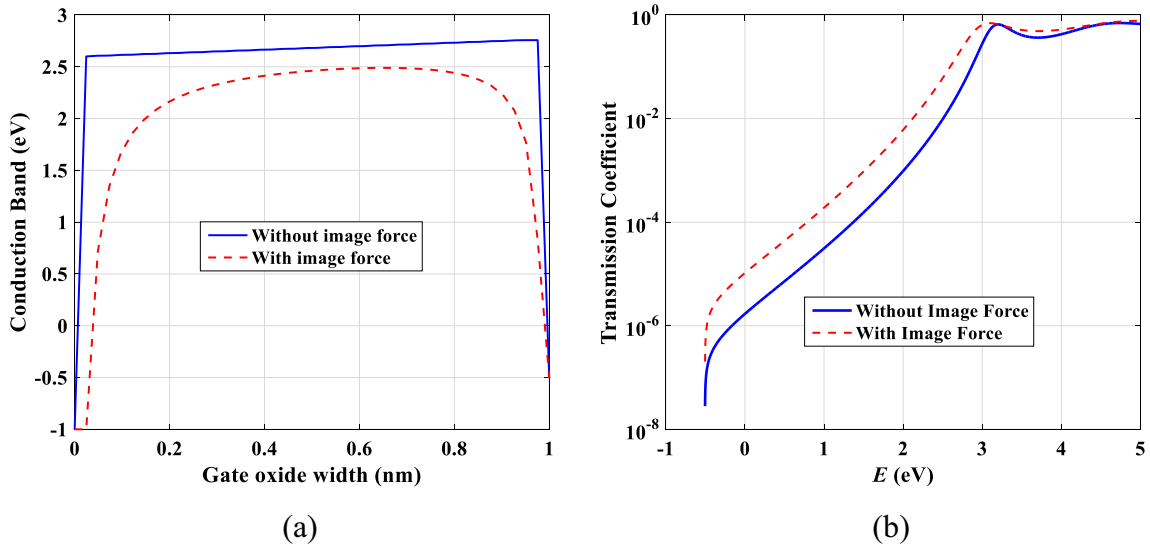

Fig. 9 The impact of the image force on both (a) conduction band and (b) transmission coefficient for $V_{DS} = 0.5$ V, $V_{GS} = 0.8$ V at $M = 25$ (mid-channel distance).

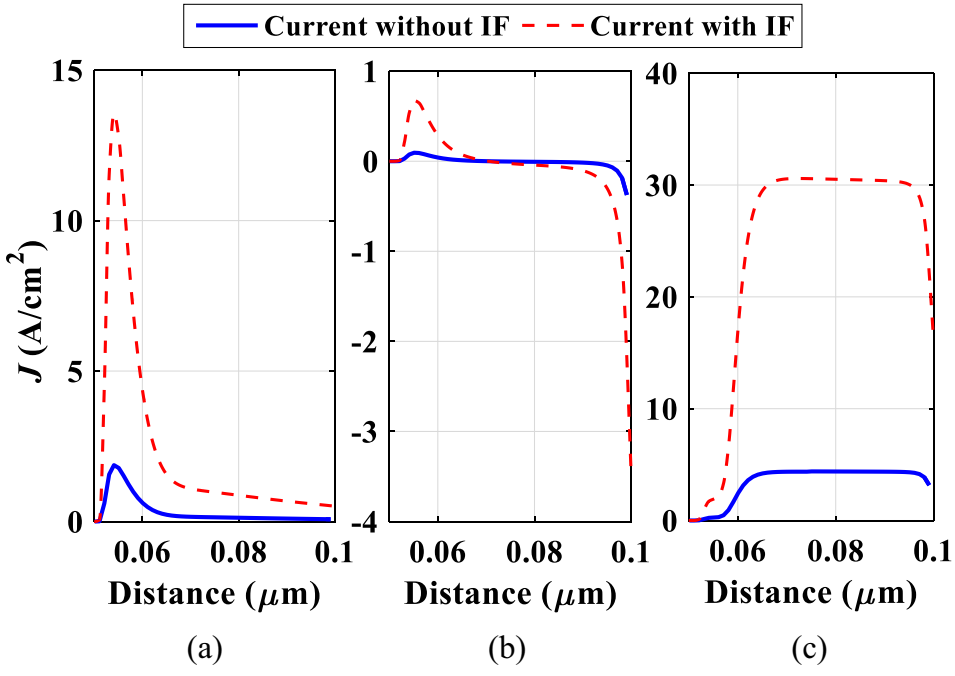

Fig. 10 Current density vs. distance along channel with and without image force (IF) for (a) $V_{DS} = 1$ V and $V_{GS} = 1$ V (b) $V_{DS} = 1$ V and $V_{GS} = 0.7$ V (c) $V_{DS} = 0.5$ V and $V_{GS} = 0.8$ V.

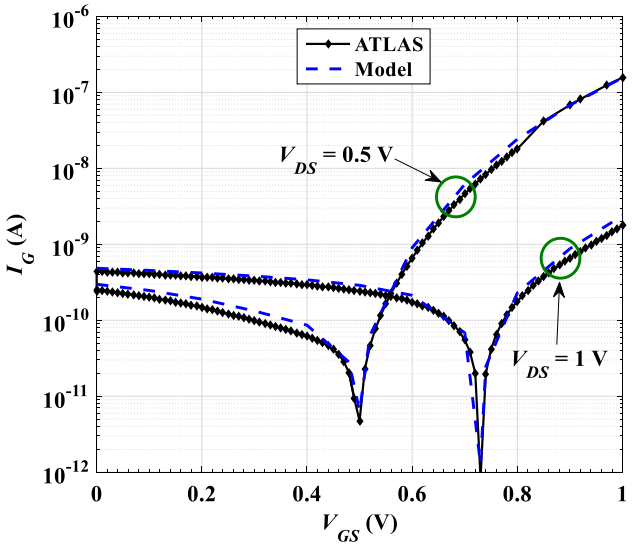

Fig. 11 Gate current vs. V_{GS} for V_{DS} = 1 V and V_{DS} = 0.5 V.

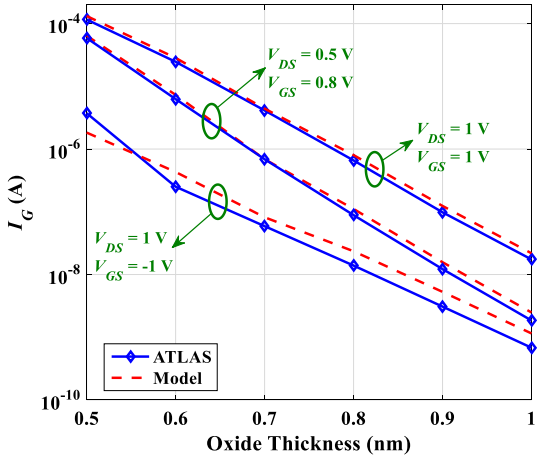

Fig. 12 Gate current vs. EOT for three cases (V_{DS} = 1 V V_{GS} = 1 V, V_{DS} = 0.5 V V_{GS} = 0.8 V and V_{DS} = 1 V V_{GS} = -1 V).

V_{DS} = 1 V and 0.5 V. The proposed semi-numerical method under analysis is found to be compliant with the TCAD simulator results with much less CPU time w.r.t. the cumbersome computational cost of the TCAD simulation. The good prediction of current levels proves the validity of the presented technique. This paves the way to using this semi-numerical method in finding the design criteria to select suitable gate oxides suitable for TFET operation.

In Fig. 12, the gate leakage current for different gate ETOs is simulated and plotted. Our technique accurately predicts the leakage current under different biases. As EOT is scaled down, the gate leakage current drastically increases. Further, the simulated I_G - V_{GS} curve is plotted in Fig. 13(a) for various thicknesses showing the gate current stepping up as the thicknesses decreases. Moreover, it is inferred from Fig. 13(b) that the ambipolarity behaviour of the TFET can be observed at negative V_{GS} values for an EOT of 1 nm and 0.5 nm. Remarkably, as the EOT decreases, both ON and OFF current increase. The ambipolar current in TFET is attenuated due to the low drain doping concentration of our structure, compared with the source. Decreasing the drain doping concentration led to a rising of both conduction and valence energy band diagram in the drain region. This causes the BTBT mechanism to lower, therefore decreasing the ambipolarity. It is obvious that the gate leakage current is the main contributor to the I_{OFF} current, and therefore its neglection can lead to an underestimation of the subthreshold swing and a higher I_{ON} to I_{OFF} ratio. Thus, it is crucial to include gate leakage currents when analysing TFET circuits to get more accurate prediction of the device performance.

It should be pointed out here that the presented physically based model is built on some assumptions and approximations that should be met in order to get reliable results. One of the main assumptions is that the TFET structure geometry does not involve overlapping, either gate-channel or drain-channel overlaps. Further, the pseudo-2D technique, employed to get the surface potential, is valid for depletion mode only. So, the drain voltage should be greater than or equal to the gate voltage. Moreover, the model is based on the supported data from TCAD simulations to

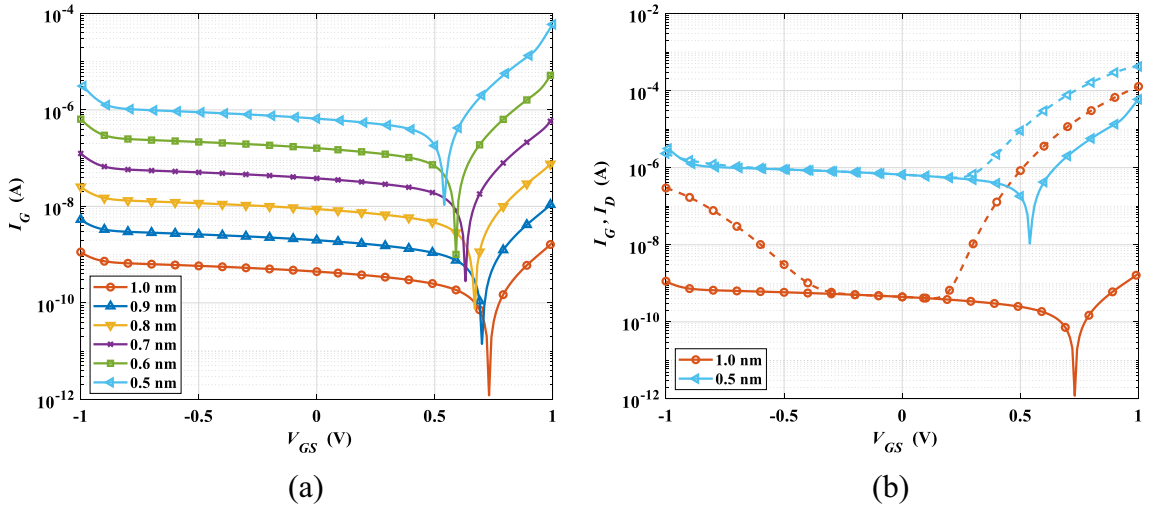

Fig. 13 Impact of different thicknesses at V_{DS} = 1 V: (a) Drain current vs. V_{GS}, (b) Drain (Dashed Line) and gate (Solid Line) current vs. V_{GS}.

get precise surface potentials through the proper fitting of the fringing effect. The model can be modified to include the impact of overlapping by extending the pseudo-2D method to be solved in four regions instead of three. However, to solve for drain voltages less than the gate voltage, the pseudo model will not be valid, and more advanced models should be incorporated. Finally, to get rid of the fitting parameters, more efforts are needed to model the fringing effect to be a unified function of bias.

5. Conclusion

In this work, the TFET gate current leakage numerical analysis through a single dielectric oxide has been thoroughly analyzed. The surface potential is accurately modeled using an analytical Pseudo-2D method that is valid for drain voltages greater than or equal to the gate voltage to ensure depletion mode. The conduction band through the oxide has therefore been successfully deducted. The gate current densities have been examined by applying TLM while taking into consideration the effect of image force.

It has been shown that the TLM numerical method accurately predicts the exact value of the gate oxide leakage current for different biasing and gate effective oxide thicknesses of the device. The error percentage for the obtained gate current densities have been found to be as low as 10%. Upon inspection, the barrier lowering due to the accumulation of image charge must be taken under account, since its neglection leads to underestimated current density values.

Simulations performed over a range of small EOTs shows the necessity of the gate leakage inclusion to obtain a correct I_{OFF} for the TFET device, since for an EOT of 0.5 nm, the gate current has been found to range from 3.5×10^{-6} A to 6×10^{-5} A for $V_{DS} = 1$ V. This indicates the necessity of its addition for an accurate subthreshold swing calculation. The validity of the numerical techniques is performed by comparing the results with TCAD simulation showing good agreement with much less CPU times regarding the presented method. In our future work, we will handle the design of gate stacks suitable for TFET low power operation to reach an optimum choice from materials and performance perspectives.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Appendix A. The following equations are extracted from REF [26]. Given a certain potential barrier, the complex propagation constant can be calculated as,

$$\gamma = j\sqrt{\frac{2m^*}{\hbar^2}(E - V)} \tag{A1}$$

Then, the characteristics impedance is computed from,

$$Z_o = \frac{\gamma\hbar}{jm^*} \tag{A2}$$

Now, the input impedance Z_{in} for a transmission line at a distance a from the load is given by,

$$Z_{in} = Z_o \frac{Z_L - Z_o \tanh(\gamma a)}{Z_o - Z_L \tanh(\gamma a)} \tag{A3}$$

The reflection coefficient for the potential barrier is calculated by utilizing $Z_{o,1}$ as the characteristic impedance and Z_1 as the load impedance,

$$\Gamma = \frac{Z_L - Z_o}{Z_L + Z_o} \tag{A4}$$

Finally, the quantum transmission probability is provided by,

$$T(E) = 1 - |\Gamma(E)|^2 \tag{A5}$$

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