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Enhancement of device characteristics of CNT-TFET: Role of electrostatic doping and work function engineering

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ABSTRACT

In this work, an Electrostatic Doped Carbon Nanotube Tunneling FET (ED CNT-TFET) has been designed and simulated using a work function engineering technique. An intrinsic CNT is introduced as a channel material and a doped pocket is created between the source and the channel by utilizing an appropriate work function to boost the ON-state current of the device. Moreover, dielectric pocket engineering is applied to boost the high-frequency performance. The simulations, performed in this work, are conducted through a 2D solution of Poisson and Schrodinger equations which are done by utilizing the unbalanced Green function formalism. Simulation results demonstrate that the proposed device structure could improve the ON-current, cut-off frequency, and achieve a low subthreshold swing (SS) value which makes it suitable for low power applications. Additionally, the presented structure could also eliminate ambipolar conduction.

1. Introduction

Carbon nanotubes (CNTs) are quasi one-dimensional nanostructures that are good candidates to be used as a channel region in field effect transistors (FETs) and replace bulk silicon. CNTs are distinguished by their ballistic conduction, superior carrier mobility, and rapid switching speeds [1-3]. One of the most promising devices, dedicated to low power applications, is the tunneling field effect transistor (TFET). It is a promising candidate for overwhelming the scaling issues encountered in traditional metal oxide semiconductor FETs (MOSFETs) [4]. The TFET operation is based on the band-to-band tunneling (BTBT) process. Because TFETs can eliminate the thermionic carrier injection to the channel in the subthreshold region, they can accomplish a subthreshold swing (SS) lesser than 60 mV/dec at room temperature [5]. This concept makes TFETs regarded as powerful candidates for future low-power devices [6-9].

However, TFETs suffer from some drawbacks regarding CMOS circuit applications [10,11] like low ON current (I_{ON}) and ambipolar conduction (I_{amb}). The reduction of I_{ON} comes from BTBT mechanism of current transport. The ambipolar conduction is the appearance of drain current when both polarities of gate voltage are applied which limits the TFET usage as a switching device. So, several techniques have been suggested to alleviate this undesired ambipolar phenomenon such as asymmetric drain/source doping, gate/drain overlap or underlap, nonuniform drain doping, spacer engineering, and gate oxide material engineering [9,12-15]. A lot of these techniques can reduce I_{amb} under certain conditions but are unable to entirely suppress this current. For enhanced ON-Current, many methods are investigated for this purpose. A design of a MOSFET that is paralleled with a TFET was studied to increase the current with the aid of work function engineering in the gate to enhance tunneling [16]. Gate-all-around field-effect transistor (GAA-FET) architecture is used for better charge control. Further, a GAA device with a silicon channel utilizing a sectorial cross-section was investigated [17]. Moreover, semi-analytical techniques have been conducted to model double-gate TFETs by utilizing a pseudo-2D approach that includes the effects of the depletion

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regions [18]. However, the ON current of TFETs needs to be boosted. Additionally, these techniques have some shortcomings including, for instance, the overall capacitance deterioration, and these drawbacks can cause serious issues in future TFET operations.

In our current work, we try to fix the aforementioned problems by using electrostatic doping (ED) with metal work function (φ) engineering. ED is a methodology in which electrons or holes are induced in semiconductors because of its band alignment nearby its interface with other semiconducting or conducting materials [19-21]. For an n-type doped semiconductor, the work function of the metal φ_m is greater than that of the semiconductor φ_s while $\varphi_m < \varphi_s$ for p-type. ED theoretically offers extremely sharp junctions having a well-controlled profile of the carrier concentration profile and keeping a low defect density as well. These characteristics make ED an appealing substitute for conventional doping profiles for a wide range of semiconductor devices. However, their ON current are not high enough and ambipolar conduction is better to be handled. A technique based on a dual-material source-gate (DMSG) structure was proposed to enhance the performance of a junctionless CNT TFET [22]. Another approach used to activate the source region is achieved by introducing a SiO_2 spacer in the HfO_2 gate dielectric, between the main gate and the P-gate [23].

In this current study, electrostatic doped CNT Tunneling field effect transistor (ED CNT-TFET) with engineering metal work functions is proposed. To enhance the ON-current, a pocket is added with an appropriate work function and adjustable length between the source and the channel. Our work is devoted to designing TFET-transistor using CNT as a channel based on electrostatic doping. The originality of our work is introducing a metallic pocket on the source side to enhance the ON/OFF current ratio. By adopting the work function of the pocket, we got an improvement in the ON/OFF current ratio by about 4 times without deterioration in the SS. Simulation techniques are carried out by the solution of non-equilibrium Green's function (NEGF) self consistently along with Poisson's equation. Details of our developed simulator are presented in [24-29]. Moreover, the calibration of this simulator against various reported measurements showed accepted validity to examine the device performance [24,25].

The remainder of the paper is structured as follows. Section 2 addresses the device architecture and the simulation setup. The influence of decreasing the difference between the work functions of the gate metal and the drain electrode on ambipolarity is presented in sec 3.1. Sec. 3.2 discusses the influence of adding a metallic pocket on the ON current. The cutoff frequency of the device is investigated in sec 3.3.

2. Device structure and simulation setup

Cross-sectional and 3D views of the conventional CNT-TFET and ED CNT-TFET with a designed pocket are presented in Fig. 1(a) and Fig. 1(b), respectively. The parameters used for carrying out the simulations are listed in Table 1. The simulation of the proposed structure is performed by using a 2-D quantum simulator under MATLAB environment [30,31]. Poisson's equation is solved in radial and transport directions self-consistently with NEGF till reaching a certain accuracy. This is utilized by employing a tight-binding Hamiltonian through a decoupled mode-space method [32,33]. An approach to calculating the electron density from Green's function is applied by implementing a recursive algorithm [34]. The transport mechanism in the channel is assumed to be ballistic which means neglecting phonon scattering in the intrinsic channel

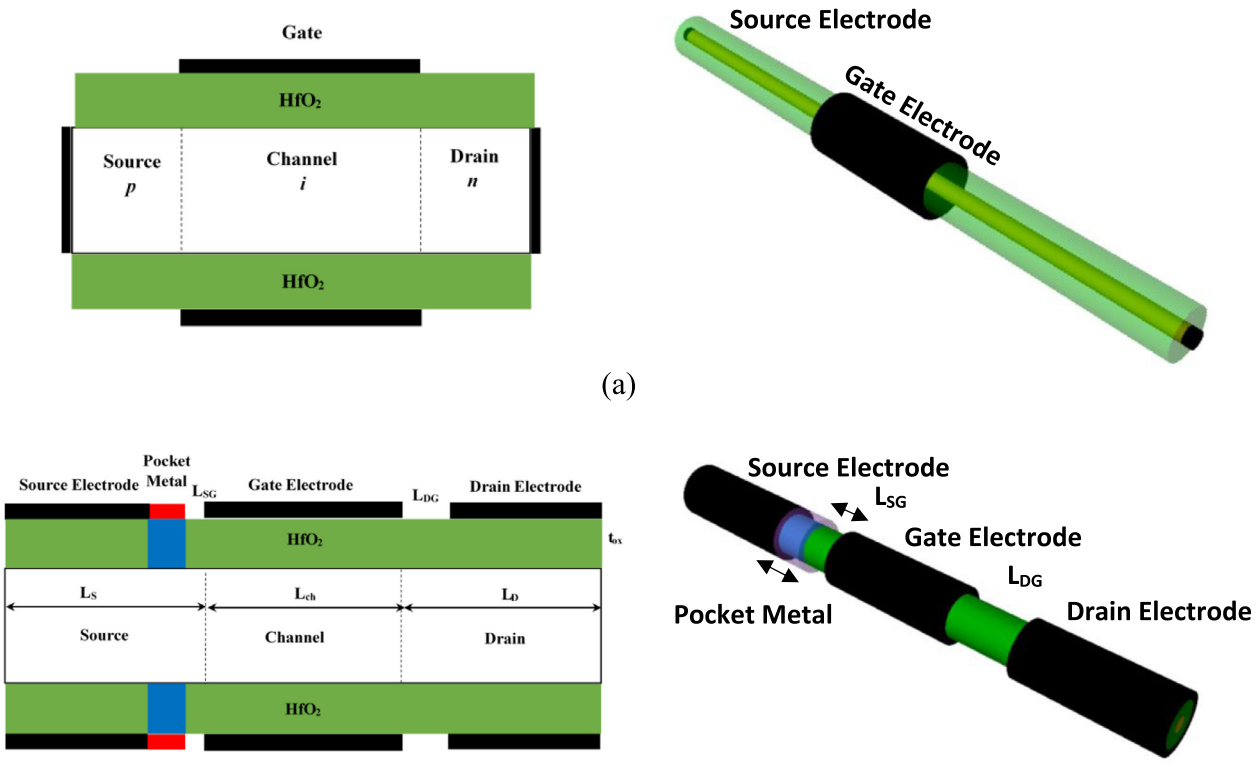

Fig. 1. Cross-sectional and 3D views of (a) conventional CNT-TFET and (b) proposed ED CNT-TFET structure.

Table 1
Physical and technological parameters of the CNT-TFET and ED CNT-TFET structures.

Device Parameters	TFET Structure	
	CNT-TFET	ED CNT-TFET
CNT type	zigzag (13,0)	zigzag (13,0)
CNT diameter	1 nm	1 nm
Channel length	20 nm	20 nm
Source/drain region length	30 nm	30 nm
Pocket Length		5 nm
Source/drain doping	1/nm	
Gate dielectric constant	16	16
Gate dielectric thickness	2 nm	2 nm
Gate work function	4.4 eV	4.4 eV
Source work function		5.4 eV
Drain work function		4.13 eV
Pocket work function		2.4 eV
L_{SG} and L_{DG}		2 nm and 5 nm

for room temperature operation where the hot phonon effect is minor [35,36]. The ballistic transport has been adopted in order to highlight the optimal limit of performance that the CNT tunnel FET can provide. Our group studied the effect of phonon scattering in the p-i-n transistor using Butticker probes. The simulated results proved that it has a minor effect on the device performance [28]. Finally, by using Landauer equation, the drain current I_D is determined. The main steps are summarized as shown in the flowchart in Fig. 2.

3. Results and discussion

The ability of the transistor to work as a switch in logic circuits depends on the ON and OFF currents. A comparison between the performances of different four structures is conducted. The first one is the conventional CNT-TFET. Another structure is ED CNT-TFET with symmetric difference between the gate metal work function and the source/drain electrodes. The source and drain

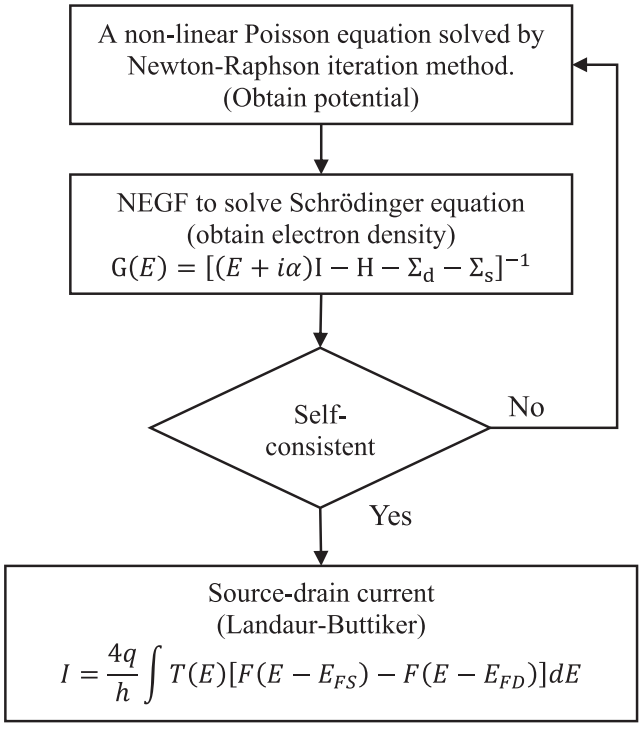

Fig. 2. Flowchart for simulation procedures showing various steps within the NEGF formalism.

metal work functions are φ_{CNT} ± 1 eV, respectively where φ_{CNT} is the work function of CNT. The third structure is the symmetric ED CNT-TFET with an introduced metallic pocket between the source and the gate with an appropriate work function. The last structure is the proposed one where the difference between the work functions of the drain and the gate is much less than that between the source and the gate with a metallic pocket at the source side. The simulation results of the transfer characteristics ($I_{DS} - V_{DS}$) for the four studied structures are presented in Fig. 3.

It can be inferred from Fig. 3 that the conventional CNT-TFET is found to undesirably have the lowest ON current (I_{ON}) and the highest ambipolar conduction. The symmetric ED CNT-TFET performance does not differ a lot from that of the conventional CNT-TFET regarding the I_{ON} and the ambipolarity. However, it has a much lower I_{ON}/I_{OFF} ratio. Inserting the metallic pocket remarkably boosts the ON-current and also lowers the ambipolarity to some extent. I_{ON} is found to be increased 14 times at V_{GS} = 0.4 V compared to the conventional CNT-TFET. For the proposed structure, in addition to the boosted ON-current, it possesses an extensively suppressed ambipolar current which supports the functionality of the device as a switch as it toggles between the ON and OFF states.

3.1. Influence of increasing the work function of the drain metal on ambipolarity

The effect of varying the work function of the drain metal is investigated to modulate the electrostatics at the drain/channel junction which controls the ambipolarity. The tunneling width at the drain-channel junction is required to be as large as possible to decrease the possibility of the BTBT of carriers at the drain side from the conduction band of the drain side to the valence band of the channel region when a negative V_{GS} is applied. The ambipolar current I_{amb} is calculated at V_{GS} = − 0.2 and V_{DS} = 0.4 V. Fig. 4 shows the band diagram of both symmetric structure having φ_S = 5.4 eV, φ_{CNT} = 4.4 eV and φ_D = 3.4 eV, and an asymmetric structure having φ_S = 5.4 eV, φ_{CNT} = 4.4 eV, φ_D = 4.13 eV. The symmetric structure shows a narrower tunneling width in Fig. 4(a) than that of the asymmetric structure presented in Fig. 4(b). The drain metal electrode with a small work function in the symmetric structure introduces holes with high concentration and the drain becomes a

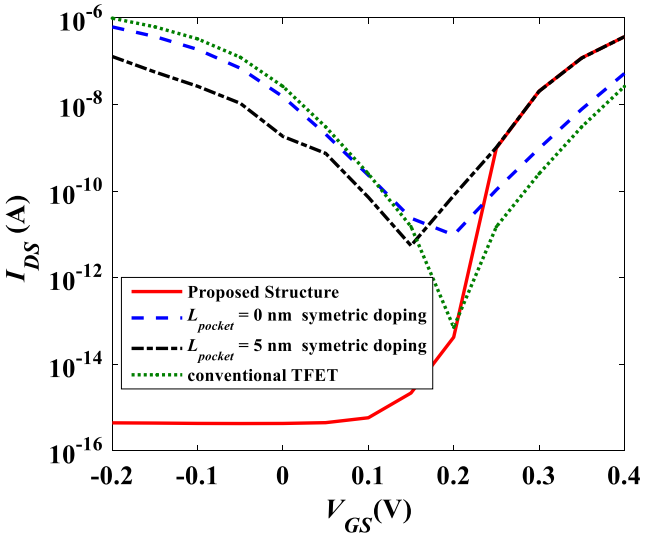

Fig. 3. The transfer characteristics of the four different structures, conventional CNT-TFET, symmetric ED-TCNTFET, symmetric ED-TCNTFET with introduced metallic pocket, and the proposed asymmetric ED-TCNTFET with pocket, calculated at V_{DS} = 0.4 V.

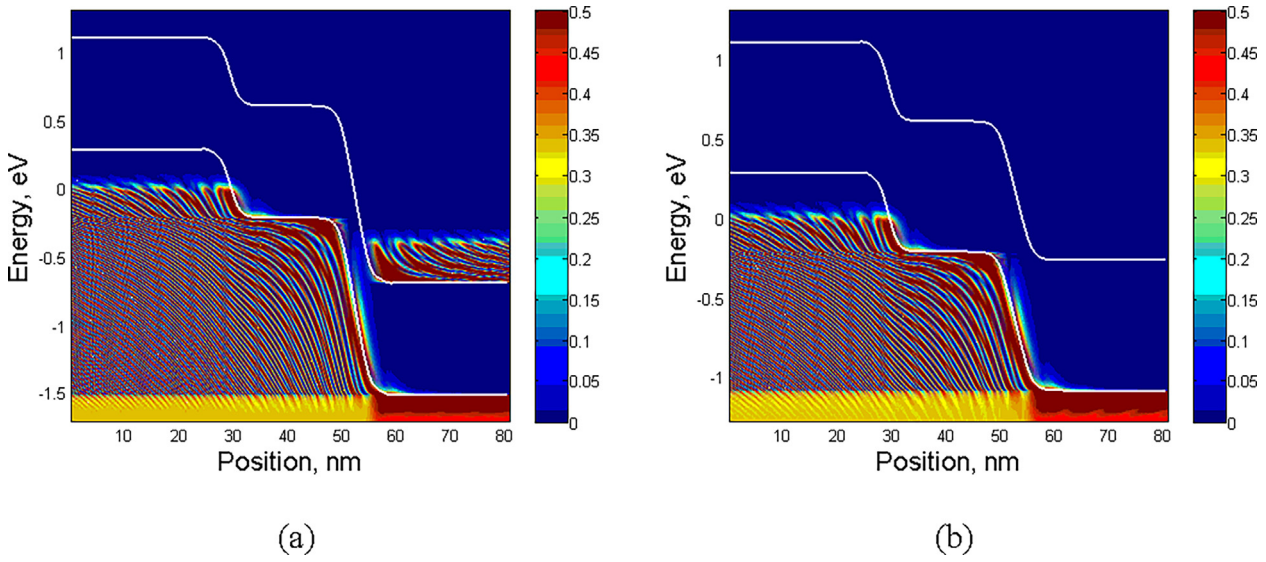

Fig. 4. LDOS and energy band diagrams of (a) symmetric structure (φ_S = 5.4 eV, φ_{CNT} = 4.4 eV, φ_D = 3.4 eV) (b) asymmetric structure (φ_S = 5.4 eV, φ_{CNT} = 4.4 eV, φ_D = 4.13 eV), showing the tunneling width between the channel valence band and the drain conduction band at V_{GS} = − 0.2 V and at V_{DS} = 0.4 V.

highly doped region. On the contrary, the increased work function of the drain metal electrode in the asymmetric structure led to less band bending and the tunneling width increased from 4.4 nm to 8 nm. Hence, the decreased difference between the work functions of the gate-drain metals results in an increased barrier width and a more suppressed ambipolar current.

To have an overall insight into the effect of the work function of the drain metal on the ambipolar current, φ_D is varied from 3.4 eV to 4.3 eV. The results are plotted in Fig. 5 and give the range in which the variation of φ_D does not influence the I_{amb}. The value of φ_D of 4.2 eV is near that of φ_{CNT} of 4.4 eV and is enough to increase the barrier width and highly suppress I_{amb}.

3.2. Influence of adding a pocket metal on ON-current

A higher possibility of BTBT of charge carriers from the conduction band of the source region to the valence band of the channel region can be achieved with a narrower tunneling width at the source/channel junction. For this purpose, a pocket metal is inserted above a part of the source. A pocket is a metal with a different work function than that of the other metal above the source (see Fig. 1(b)). The ON-current I_{ON} is determined at V_{GS} = V_{DS} = 0.4 V. Fig. 6 shows the band diagram of the asymmetric structure having φ_S = 5.4 eV, φ_{CNT} = 4.4 eV, φ_D = 4.13 eV, and the effect of adding the pocket with φ_{pocket} = 2.4 eV is examined. The structure without a pocket has a wider tunneling barrier in Fig. 6(a) than that of the structure with a pocket shown in Fig. 6(b). The inserted pocket metal with an extensively small work function leads to more bending of the energy band beneath the pocket and an increase in the possibility of the BTBT since the tunneling width decreased from 3.6 nm to 1.3 nm, and hence I_{ON} is boosted.

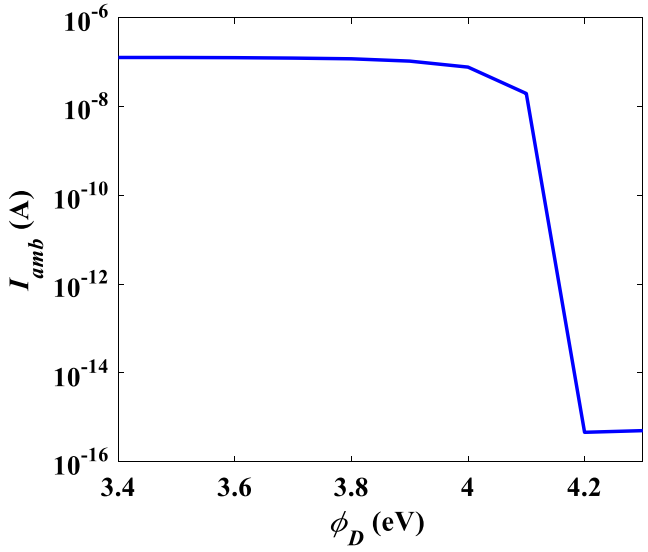

Fig. 5. Influence of the metal work function at the drain side on the ambipolar current I_{amb} at V_{GS} = − 0.2 V and at V_{DS} = 0.4 V.

Moreover, φ_{pocket} is varied from 3 eV to 5 eV to examine its effect on I_{ON}. Lower values of φ_{pocket} give higher values of I_{ON} as expected. The lowest value of I_{ON} occurs when φ_{pocket} = φ_{CNT} = 4.4 eV as presented in Fig. 7.

3.3. High-frequency response of the different structures

One of the most crucial parameters for RF circuitry is the cutoff frequency f_T [37,38]. f_T is required to be high, and this implies high transconductance and low capacitance. The cutoff frequency calculated at V_{DS} = 0.4 V for the different studied structures is illustrated in Fig. 8 where it is defined as,

$$f_T = \frac{1}{2\pi}\frac{g_m}{C_G} \tag{1}$$

Where g_m is the transconductance while C_G is the total gate capacitance which is determined from,

$$C_G = \frac{\partial Q_G}{\partial V_{GS}} \tag{2}$$

The total gate charge Q_G for a tube of radius R and channel length L_g and a permittivity $\varepsilon_r\varepsilon_o$ is calculated as,

$$Q_G = 2\pi R \int_{L_g} \varepsilon_r\varepsilon_0 E(x) \tag{3}$$

Where $E(x)$ is the axial component of the electric field along the x-direction. The proposed structure is found to have the highest f_T where it increases about 2.3 times compared to the conventional CNT-TFET as depicted in Fig. 8.

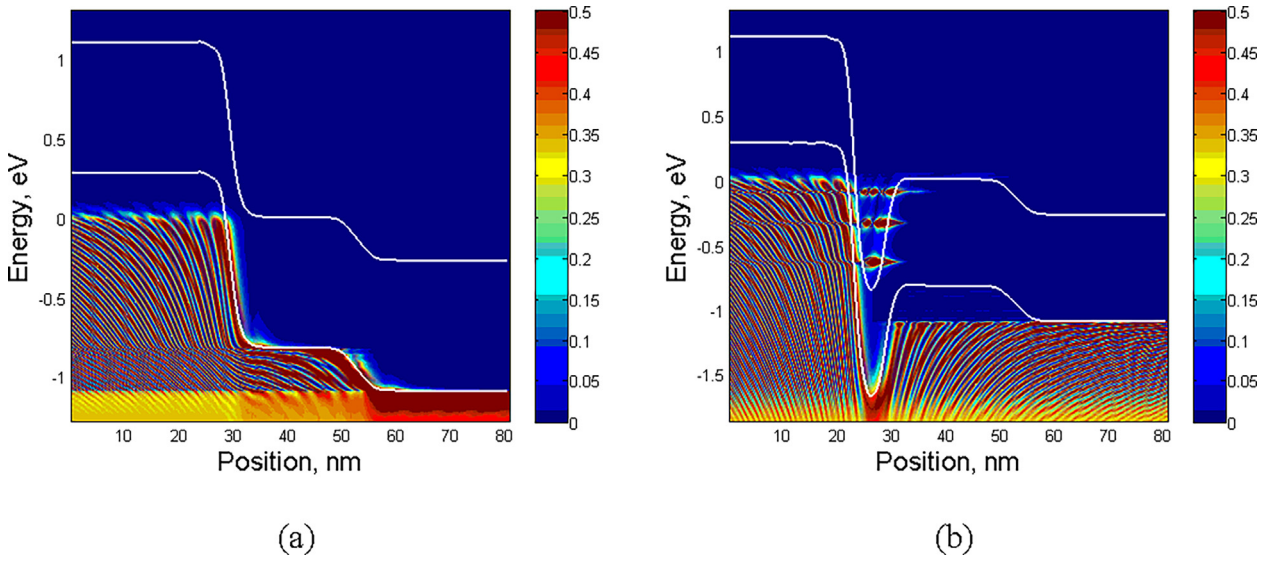

Fig. 6. LDOS and energy band diagrams of asymmetric structure (φ_S = 5.4 eV, φ_{CNT} = 4.4 eV, φ_D = 3.4 eV) (a) with L_{pocket} = 0 (b) with L_{pocket} = 5 nm and φ_{pocket} = 2.4 eV, showing the tunneling width between the source valence band and the channel conduction band at V_{GS} = V_{DS} = 0.4 V.

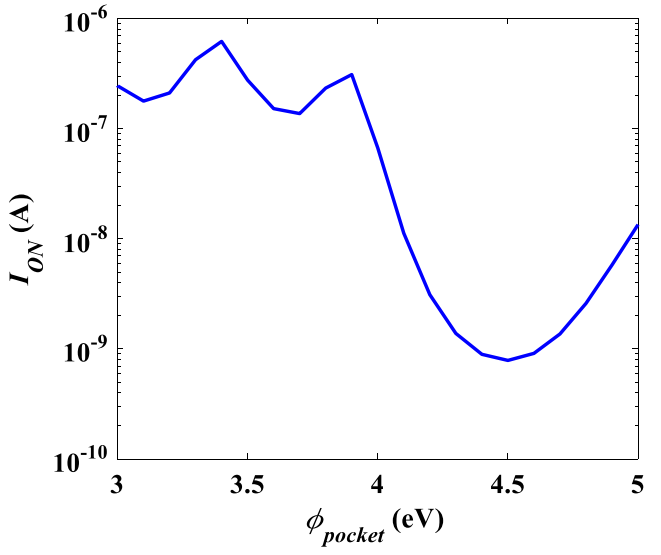

Fig. 7. Impact of the metal work function at the source region on the ON current I_{ON} at V_{GS} = V_{DS} = 0.4 V.

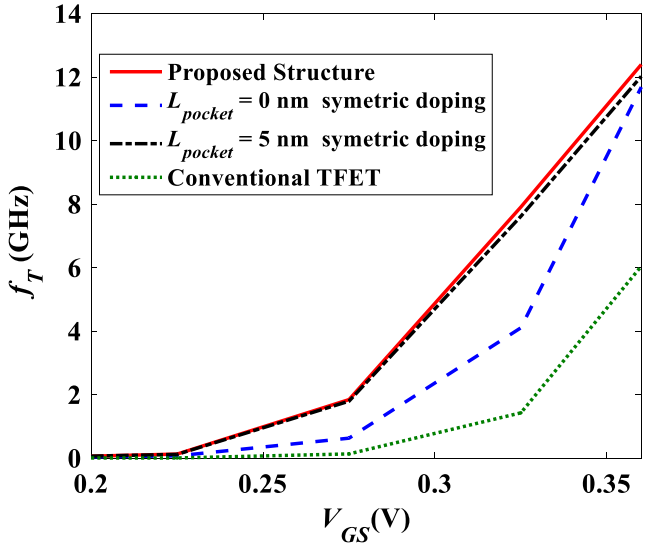

Fig. 8. Cutoff frequency of the different structures, conventional CNT-TFET, symmetric ED CNT-TFET, symmetric ED CNT-TFET with introduced metallic pocket, and the proposed asymmetric ED CNT-TFET with pocket, calculated at V_{DS} = 0.4 V.

To explain the behavior of the cutoff frequency (f_T) of the device, the transconductance, and the gate capacitance should be studied in detail. The simulation results for C_G with respect to the gate-source voltage at V_{DS} = 0.4 V are shown in Fig. 9(a). The capacitance of the symmetric ED CNT-TFET structure is found to be almost the same as that of the conventional TFET. On the contrary, both the symmetric and asymmetric structures with an introduced pocket of L_{pocket} = 5 have a higher capacitance. The proposed structure has C_G that is 6 times that of the conventional TCNTFET. Regarding the transconductance g_m, the different structures have the same tendency as that found for the capacitance where the proposed structure has higher values as illustrated in Fig. 9(b). However, the rise in g_m is much greater where it increased 14 times for the proposed structure compared to the conventional CNT-TFET. The high increase of the transconductance compared to the small increase in gate capacitance leads to an overall increase in the cut-off frequency of the device.

3.4. Influence of inserting dielectric pocket on different device parameters

For a higher better device performance, a dielectric pocket is added below the pocket metal. The effect of the presence of the pocket dielectric on the drain current is first investigated. The pocket dielectric constant k_{pocket} is varied from 4 to 24. Fig. 10(a) presents the increase of the I_{ON} with increasing k_{pocket}. This could be explained according to the decreased tunneling width. It can be depicted from the figure that an optimum value for the k_{pocket} to give the highest I_{ON} is about 21. This gives I_{ON} about double its value in case of the absence of the pocket dielectric with k = 20. Next, the influence of the existence of the dielectric pocket on the cutoff frequency is examined. The same tendency occurs as f_T increases with increasing k_{pocket} giving an optimal value for k_{pocket}

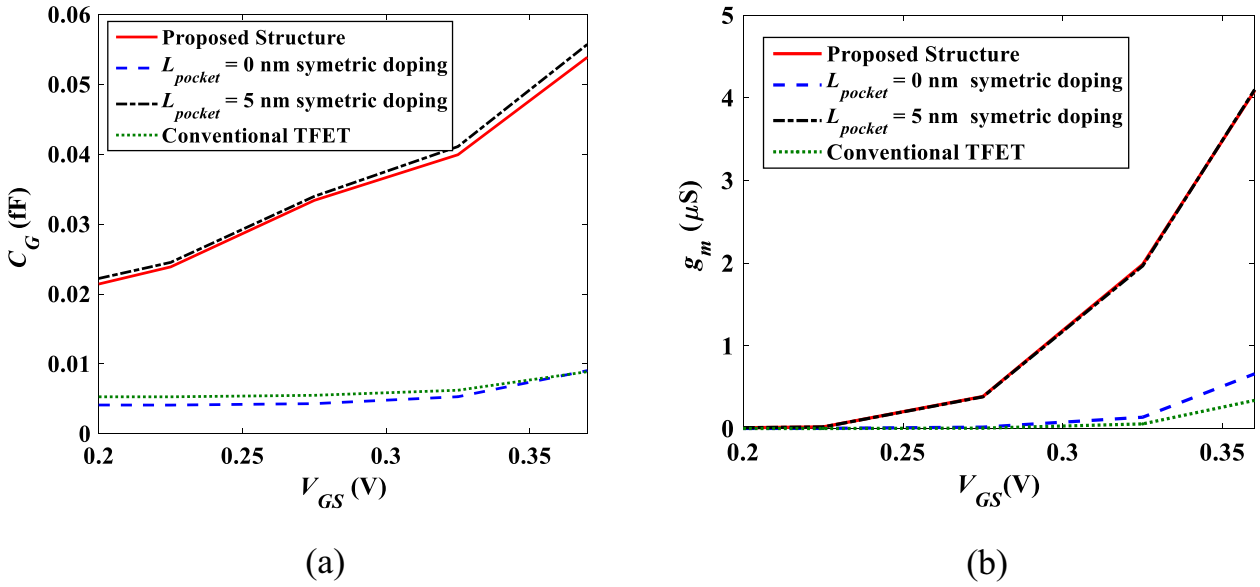

Fig. 9. (a) The overall gate capacitance C_G (b) Transconductance of the different structures, conventional CNT-TFET, symmetric ED CNT-TFET, symmetric ED CNT-TFET with introduced metallic pocket, and the proposed asymmetric ED CNT-TFET with pocket, calculated at V_{DS} = 0.4 V.

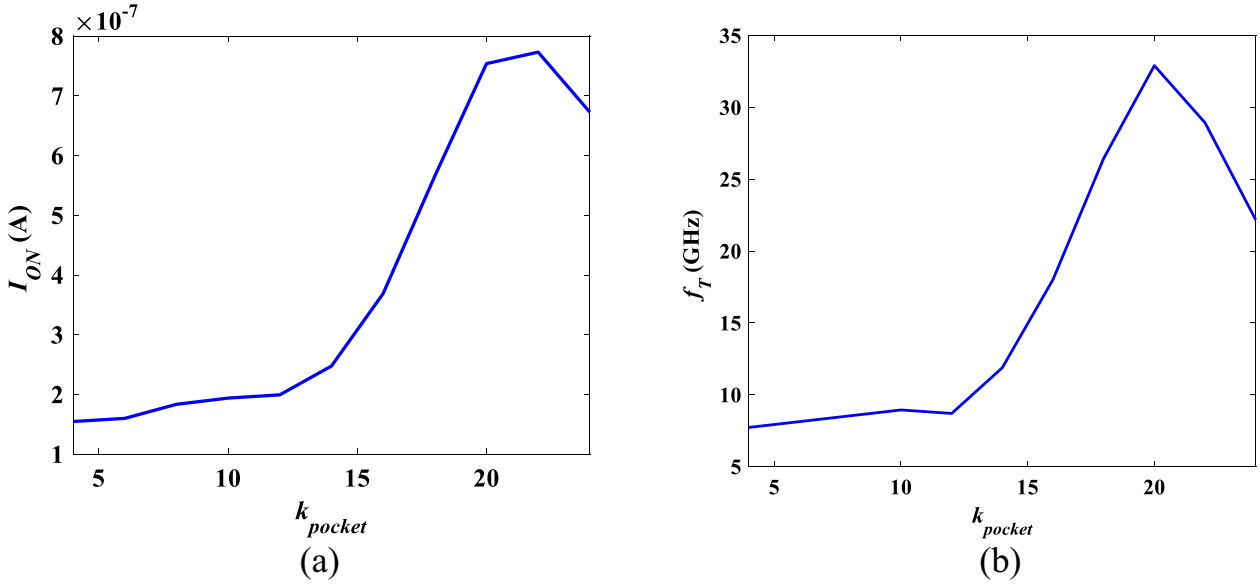

Fig. 10. Influence of the dielectric constant of the pocket dielectric k_{pocket} at the source side (a) on the ON current I_{ON} (b) on the cutoff frequency f_T, both at V_{GS} = V_{DS} = 0.4 V.

of about 20 as in Fig. 10(b). Hence, the f_T value can be doubled with this pocket dielectric. For a closer look, both the I_{ON} and f_T are examined for certain values of k_{pocket} of 16 and 20. Fig. 11 shows the increased values of I_{ON} and f_T where both are almost doubled for k_{pocket} = 20 compared to k_{pocket} = 16 at V_{GS} = 0.4 V.

Again, to explain the tendency of the cutoff frequency, the gate capacitance and the transconductance are studied for the same values of k_{pocket} as indicated in Fig. 12. The results show that the gate-source capacitance undesirably increases about 1.6 times at V_{GS} = 0.4 V when using k_{pocket} = 20 instead of 16, while the transconductance increases about 2.5 times under the same conditions. However, the higher increase in the transconductance compared to the increase in the source-gate capacitance gives an overall increase in f_T. Moreover, in Table 2, the main performance parameters, resulting from the simulation of the presented devices are listed. The performance parameters are calculated as follows. I_{ON} is computed at V_{GS} = 0.4 V and V_{DS} = 0.4 V and I_{OFF} is quantified at V_{GS} = 0.2 V and V_{DS} = 0.4 V, while I_{amb} is calculated at V_{GS} = − 0.2 V and V_{DS} = 0.4 V. The *SS* is assumed to be the average *SS* [12].

Finally, in Table 3, we represent a comparison of our proposed structure metrics with previously published doping-less structures. It can be realized from the given table that, in comparison to previously published studies [39-42], our proposed structure could simultaneously have a relatively higher ON-current and lower subthreshold swing.

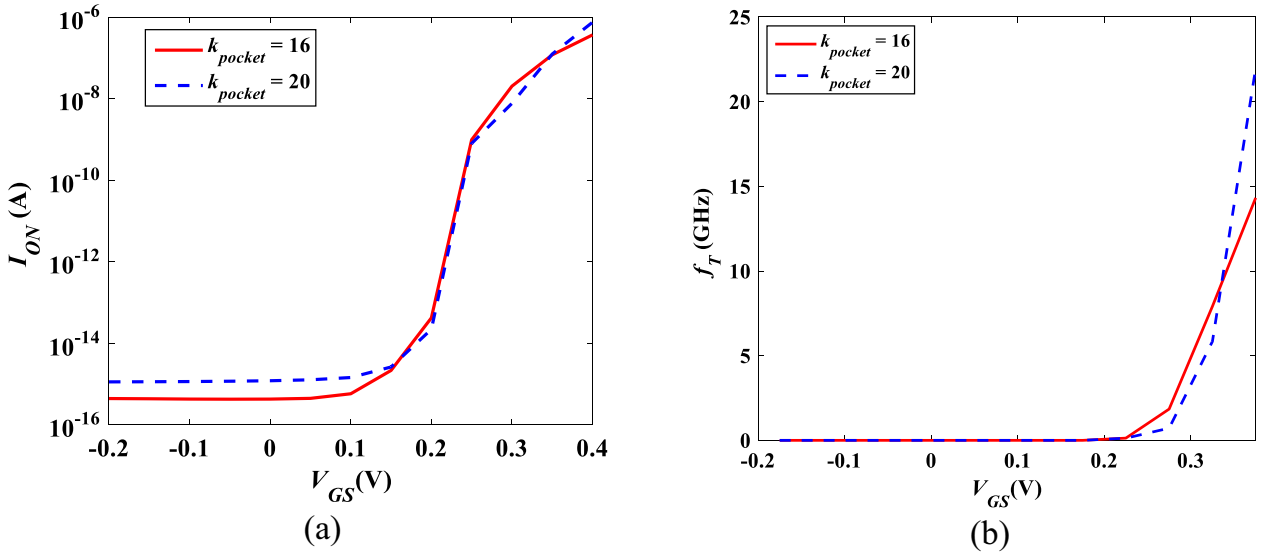

Fig. 11. (a) The ON current I_{ON} and (b) the cutoff frequency f_T of the device for two values of k_{pocket}, 16 and 20.

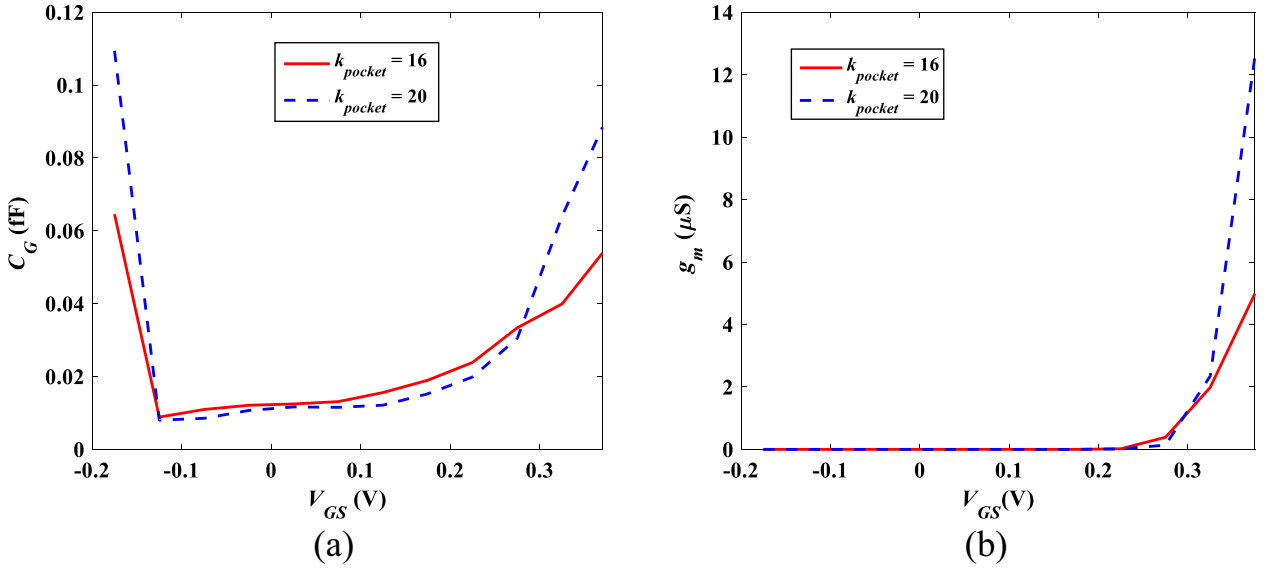

Fig. 12. (a) The overall gate capacitance C_G and (b) the transconductance g_m of the device for two values of k_{pocket}, 16 and 20.

Table 2
Various output parameters for the different structures.

Structures	Parameters					
	I_{ON} (μA)	I_{OFF} (pA)	I_{ON}/I_{OFF}	SS (mV/dec)	I_{amb} (μA)	f_T (GHz)
Conventional CNT-TFET	2.62×10^{-2}	7.12×10^{-2}	3.69×10^{5}	40.85	9.89×10^{-1}	8.0
Symmetric ED CNT-TFET	5.21×10^{-2}	9.67	5.38×10^{3}	52.33	6.22×10^{-1}	13.6
Symmetric ED CNT-TFET with introduced metallic pocket	3.69×10^{-1}	78.9	4.67×10^{3}	38.58	1.29×10^{-1}	13.9
Proposed Structure	3.69×10^{-1}	4.20×10^{-2}	8.80×10^{6}	36.43	4.4×10^{-10}	14.3
Proposed Structure with dielectric pocket	7.54×10^{-1}	2.20×10^{-2}	3.43×10^{7}	36.43	1.13×10^{-10}	22.0

Table 3
Comparison of different doping-less TFET.

Ref.	Doping-less Structure	Dimensions	I_{ON} (A)	I_{OFF} (A)	I_{ON} / I_{OFF}	SS (mV/ dec)
[22]	junctionless carbon nanotube tunneling FETs using dual material source gate	d = 0.782 nm (10,0), L_G = 5 nm, t_{ox} = 2 nm	$\sim 10^{-7}$	$\sim 10^{-11}$	$\sim 10^{4}$	29 (SS_{min})
[23]	(CNT-JLTFET) based on the charge plasma concept with a combination of high-k and low-k gate dielectric	d = 1 nm (15,0), L_G = 15 nm, t_{ox} = 2 nm	$\sim 10^{-7}$	$\sim 10^{-13}$	$\sim 10^{7}$	10.97 (SS_{min}) 35.4 (SS_{av})
[39]	DL-T-CNTFET GAA	d = 1 nm (13, 0), L_G = 20 nm, t_{ox} = 2 nm	2.87×10^{-7} (V_{GS} = 0.5 V, V_{DS} = 0.4 V)	2.96×10^{-11} (V_{GS} = 0.1 V, V_{DS} = 0.4 V)	9.7×10^{3}	34.18
[40]	ED-SBCNTFET planner double gate structures	d = 1 nm (13, 0), L_G = 20 nm, t_{ox} = 1.5 nm	5.8×10^{-6} (V_{DS} = 0.5 V, V_{GS} = 1 V)	1.02×10^{-12} (V_{DS} = 0.5 V, V_{GS} = 0 V)	5.8×10^{6}	61.3
[41]	ED-tunnel CNTFET	d = 1 nm (13, 0), L_G = 20 nm, t_{ox} = 1 nm	4×10^{-6} (V_{GS} = − 1 V, V_{DS} = − 0.6 V)	8.4×10^{-12} V_{DS} = -0.6 V, V_{GS} = 0 V	4.7×10^{5}	
[42]	Dynamically Configurable Electrostatic Doped Carbon Nanotube Tunnel FET	d = 1 nm (13,0), L_G = 20 nm, EOT = 1 nm		(Order of 10^{-18} A/nanotube) as compared to conventional CN-TFET (order of 10^{-15} A/ nanotube)	10^{13} (his conventional is 10^{9})	23.2 (SS_{min})
Our Work	ED CNT-TFET with different metal work functions and pocket	d = 1 nm (13, 0), L_G = 20 nm, t_{ox} = 2 nm	3.69×10^{-7} (V_{GS} = 0.4 V, V_{DS} = 0.4 V)	4.2×10^{-14} (V_{GS} = 0.2 V, V_{DS} = 0.4 V)	8.8×10^{6}	10.97 (SS_{min}) 36.43 (SS_{av})
Our work	ED CNT-TFET with different metal work functions and pocket and adding a dielectric pocket	d = 1 nm (13, 0), L_G = 20 nm, t_{ox} = 2 nm	7.54×10^{-7} (V_{GS} = 0.4 V, V_{DS} = 0.4 V)	2.21×10^{-14} (V_{GS} = 0.2 V, V_{DS} = 0.4 V)	3.4×10^{7}	10.97 (SS_{min}) 36.43 (SS_{av})

4. Conclusion

In this paper, a 2D quantum simulator has been used to study Electrostatic Doped Tunneling FET (ED CNT-TFET) applying various work functions and dielectric engineering techniques. A metal pocket is inserted between the source and the channel and designed in terms of work function and length to increase the ON-current by 14 times compared to the conventional TCNTFET. Moreover, the work function of the metal of the drain is appropriately chosen to suppress the ambipolar current to increase the functionality of the device to work as a switch. Besides, the cutoff frequency of the device is studied and the proposed structure is found to have about 2.3 times increased cutoff frequency compared to the conventional CNT-TFET. In addition, the proposed structure showed an enhanced subthreshold swing. Moreover, adding a pocket dielectric under the pocket metal at the source side could boost the device performance as both the ON-current and the cutoff frequency are almost doubled compared to the case of the absence of the pocket dielectric. The simulation results revealed that the proposed ED-TCNTFET can exhibit unipolar characteristics with excellent OFF state, enhancement of ON-current, and steep subthreshold slope indicating superior characteristics to be used in high-performance low-power applications.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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