Natl. Acad. Sci. Lett. (March–April 2020) 43(2):167–170
https://doi.org/10.1007/s40009-019-00830-0

SHORT COMMUNICATION

Parasitic Suppression in 2D Smart Power ICs Using Deep Trench Isolation: A Simulation Study

Mohamed Abouelatta[1] · Marwa S. Salem[2,3] · Ahmed Shaker[1] · Mohamed Elbanna[1] · Abdelhalim Zekry[1] · Christian Gontrand[4,5]

Received: 8 September 2018 / Revised: 28 September 2018 / Accepted: 22 August 2019 / Published online: 10 September 2019
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Abstract In this letter, a planar integration using the deep trench isolation (DTI) technique is proposed to suppress the inter-well parasites in smart power integrated circuits implemented in 0.35 µm BiCMOS technology. In this technology, all devices share the same epitaxial layer. This can lead to a punch-through between power devices as well as between power and low-voltage CMOS devices. A DTI scheme is used to suppress the effect of the parasitic BJT by using a P^+ retardation implant region under the deep trench isolation region. The injection ratio of the parasitic BJT is reduced by a factor between 3 and 8.5. The effect of the trench length and the retardation implant is investigated using SENTAURUS TCAD simulations. It is confirmed, through using TCAD simulations, that the amount of the collected carriers of the sensitive devices changes as a function of the trench length and the presence of the retardation implant.

Keywords Parasitic suppression · 2D smart power ICs · Deep trench isolation · 0.35 µm BiCMOS · TCAD

✉ Mohamed Abouelatta
m.abouelatta@eng.asu.edu.eg

Marwa S. Salem
marwa_asu@yahoo.com

Ahmed Shaker
ahmed.shaker@eng.asu.edu.eg

Mohamed Elbanna
mm.elbanna@eng.asu.edu.eg

Abdelhalim Zekry
aaazekry@hotmail.com

Christian Gontrand
Christian.Gontrand@insa-lyon.fr

1 Faculty of Engineering, Ain Shams University, Cairo, Egypt

2 Computer College, Hail University, Hail, Saudi Arabia

3 Modern Science and Arts University (MSA), Cairo, Egypt

4 INSA- Lyon, Villeurbanne, France

5 IEP, Université Euro-méditerranéenne de Fès, INSA- Fès, Fès, Morocco

Introduction

In smart power ICs, there are substantial improvements in performance and reliability, and reduction in cost compared to the discrete approach. The savings come from the elimination of the many packages needed to house the individual chips. However, crosstalk between power devices and the interaction between power and low-voltage devices are the most significant hurdles [1, 2]. In this letter, DTI scheme is introduced for high-voltage isolation. DTI-based processes have been integrated previously in CMOS architectures to suppress inter-well parasites and CMOS thyristor latch-up. Nowadays, this isolation scheme could be used to reduce the isolation distance between power devices as well as between power device and low-voltage CMOS devices.

Although SOI platforms are very efficient in electrical isolation and chip area reduction, the design complexity, higher wafer cost and lower heat removal capability limit the use of these technologies. The deep trench high-voltage isolation is a low-cost alternative to SOI. The deep trench isolation (DTI) is suitable for the smart power ICs implemented in BiCMOS technology. Moreover, this scheme has higher heat removal capability than SOI scheme. It reduces the isolation distance between power devices as well as between power device and low-voltage CMOS devices, thus causing a reduction in the total chip area drastically

compared to a standard junction isolation scheme [3–5]. This type of isolation is suitable for the smart power automotive ICs [6, 7].

During the development phase of the deep trench, severe silicon stress situations, which lead to defects within the silicon material, are faced. To get the complete structure free of defects, a filler material combination (oxide/polysilicon) is used [8, 9]. However, punch-through under the deep trench becomes a concern. This can be avoided in P-substrate with punch-through retardation implants (P^+ boron implant) or simply by increasing the depth of the trench significantly.

Minority carrier diffusion is a key problem in smart power ICs. The underground conditions on the output driver stage can lead to a significant electron current injection into the substrate. Negative voltages (down to − 1.5 V) occur in power stages due to inductive loads switching during normal operation (motor control in automotive applications). This causes the injection of minority carriers into the substrate, leading to their collection by sensitive N-wells in the p-channel LDMOS (pLDMOS) device or in the CMOS devices. As a result, it causes potential failures of their functionalities.

A simplified cross section, containing the complementary LDMOS (cLDMOS), CMOS and the parasitic NPN BJT, is shown in Fig. 1. In this structure, The CMOS is simplified to have only the source contacts of the MOS devices. The N^+ source contact of the nMOS and the N^+ source-body contact of the nLDMOS are tied to ground. While the P^+ source contact of the pMOS is connected to V_{DDL} (3.3 V), the P^+ source-body contact of the pLDMOS is connected to V_{DDH} (42 V) which is the new automotive battery voltage. The technological and geometrical parameters are shown in Table 1 [10, 11].

Due to the negative bias applied to the drain of the cLDMOS in Fig. 1, the N-epi/P-substrate diode becomes forward biased. It induces a large current. Most of the current is drained towards the source (S_n) through the intrinsic body diode. The remaining part of the injected current (I_E) flows into the substrate, and it can be collected by any reverse-biased junction.

The N-region of the pLDMOS at V_{DDH} acts as a collector of the lateral parasitic NPN transistor with current I_{C1}, as shown in Fig. 2. Other N-regions on a positive potential V_{DDL}, e.g. those of the controlling circuitry, also collect the minority carriers with current I_{C2}. This can disturb the functionality of its components.

In BiCMOS technology, all devices share the same epitaxial layer. This leads to crosstalk between power devices as well as between power and low-voltage CMOS devices. The injection collected ratio α, which is defined as the ratio of the collected current I_C to the injected current I_E, $\alpha = (I_C/I_E)$ reaches about 0.35. By using the deep trench isolation, this ratio is reduced by a factor between 3 and 8.5.

Insightful investigations are carried out with a TCAD device simulator because a circuit simulator does not take into consideration minority carriers. The simulations are carried out with a voltage of − 2 V applied to the drain of the cLDMOS. All the other contacts are grounded, as it is hard to characterize the structure of Fig. 1 with multi-potential levels (− 2 V, 0 V, 3.3 V, 42 V) in TCAD. This is because of the convergence problems. The injection collected ratio (α) of the most sensitive devices as a function of the trench length (L_{DTI}) is shown in Fig. 2. The

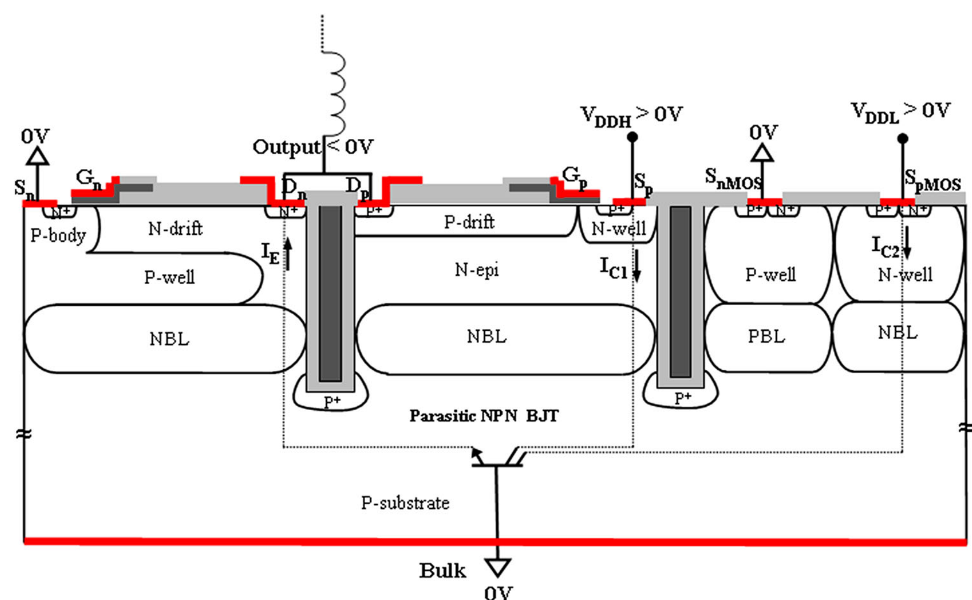

Fig. 1 Simplified cross section, showing the cLDMOS, the CMOS and the parasitic NPN transistor

Table 1 The technological and geometrical parameters of the smart power structure (*B* boron, *P* phosphorus, *As* arsenic, *W* width, *T* thickness)

	Doping	Dimensions
P-substrate	B, orientation = <100>	36 μm × 21 μm
	Conc. = 2.0×10^{15} cm^{-3}	
Epitaxy	P, conc. = 2.5×10^{16} cm^{-3}	T = 4 μm
P-body	B, dose = 2×10^{13} cm^{-2}	
P-drift	B, conc. = 1.25×10^{17} cm^{-3}	$W \approx$ 7 μm
Source/drain	As, dose = 4×10^{15} cm^{-2}	$W \approx$ 1 μm
N-buried	P, conc. = 3.5×10^{18} cm^{-3}	$W \approx$ 5 μm (pMOS)
P-buried	B, conc. = 2.5×10^{17} cm^{-3}	$W \approx$ 5 μm (nMOS)
N-well	P, conc. = 10^{17} cm^{-3}	$W \approx$ 6 μm (pMOS)
		$W \approx$ 2.5 μm (pLDMOS)
P-well	B, conc. = 1.25×10^{17} cm^{-3}	$W \approx$ 6 μm (nMOS)
		$W \approx$ 2.5 μm (nLDMOS)
P^+-isolation	As, dose = 4×10^{15} cm^{-2}	$W \approx$ 2.5 μm

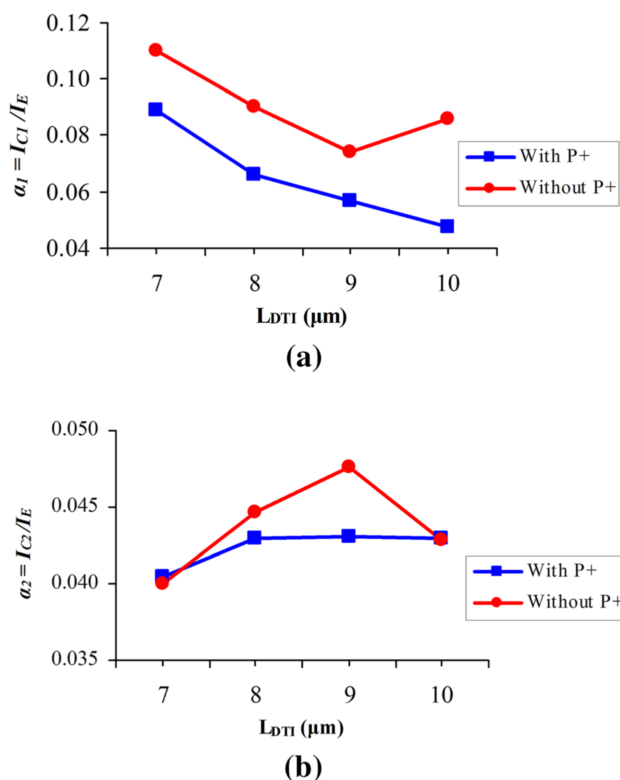

Fig. 2 Injection collected ratio in two cases with and without P^+ of **a** pLDMOS and **b** pMOS

figure indicates the injection collected ratio with and without P^+ implant.

For the first case, trench isolation without P^+ implant, α_1 decreases with the increase of L_{DTI} for $L_{\mathrm{DTI}} \leq 9$ μm. For the same range values of L_{DTI}, α_2 is increased as illustrated in Fig. 2b. For L_{DTI} = 10 μm, the situation is reversed. This means that the amount of the deflected carriers changes as a function of the trench length and the distance between the emitter and the collector regions.

For the second case, trench isolation with P^+ implant, α_1 decreases with the increase of L_{DTI} for the whole range and it is reduced by more than 23% compared to the case without P^+; α_2 is nearly constant as illustrated in Fig. 2b. As a conclusion, this highly doped implant region reduces the lifetime of the minority carriers and hence reduces the collected carriers of the sensitive devices.

A simplified smart power structure is simulated which contains nLDMOS and LV CMOS with three voltage levels (0, 3.3 V and − 5 V). In this structure, we investigate the effect of negative voltage on the drain of the nLDMOS with the presence of the retardation implant on the impact ionization rate and hence the reliability of the structure.

From Fig. 3, it can be depicted that the P^+ implant suppresses the impact ionization in the bulk of the LV devices (Fig. 3b) compared with that of the impact ionization without the P^+ implant (Fig. 3a). The impact ionization is decreased from about 10^{12} cm^{-3} s^{-1} to zero with application of the P^+ retardation implant as in Fig. 3b and reduces the bulk current significantly.

Conclusion

The deep trench isolation (DTI) is suitable for the smart power automotive ICs implemented in BiCMOS technology. This scheme has higher heat removal capability than SOI scheme. It reduces the isolation distance between power devices as well as between power device and low-voltage CMOS devices, thus causing a reduction in the total chip area. By using DTI technique with highly doped

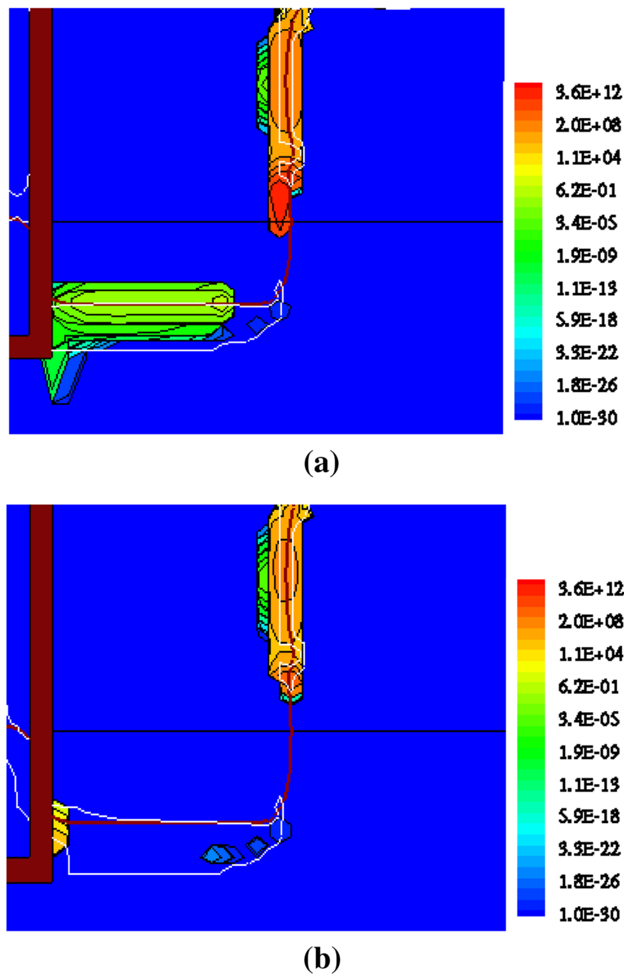

Fig. 3 Impact ionization of nLDMOS/CMOS structure **a** without P^+ implant and **b** with P^+ implant

implant region, the lifetime of the minority carriers is reduced and hence reduces the collected carriers of the sensitive devices which suppress the effect of the parasitic BJT.

Acknowledgements The authors are thankful to the UpM (Union pour la Méditerranéenne) for the collaboration and joint research work.

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