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Performance optimization of high-K pocket hetero-dielectric TFET using improved geometry design

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ABSTRACT

This study explores the optimization of a hetero-dielectric tunnel field-effect transistor (HDTFET) structure to improve device performance. By incorporating a high-k oxide pocket in a portion of the source-side gate insulator, a local minimum in the conduction band edge is induced at the source-channel interface. This technique leads to improved tunneling rates and increased current handling capability. The simulation analysis focuses on optimizing the position and dimension of the high-k dielectric pocket to enhance key device characterization metrics such as ON-state current (I_{ON}), ON-to-OFF-state current ratio (I_{ON}/I_{OFF}), subthreshold swing (SS), and cutoff frequency (f_T). The resulting optimized design for a 30 nm-channel length involves a pocket shift of 1 nm and a pocket length of 12 nm. This configuration achieves a remarkable ON current of 55 μA/μm, which is 30 times higher than that of a conventional TFET. Importantly, other analog performance parameters remain unaffected, with f_T surpassing 175 GHz for the 30 nm-channel. Additionally, transient analysis is conducted by applying a resistive load inverter circuit to a pulse input. The fall propagation delay (t_{phl}) exhibits a greater than two orders of magnitude enhancement, along with improved overshoot voltage (V_P) compared to a TFET without a pocket. The study further explores the impact of supply scaling on transient parameters. Optimal pocket scalability concerning channel length is found to be 40% for pocket length and approximately 2.5% for pocket shift relative to the source-channel interface. The proposed design significantly enhances DC and analog as well as circuit-level metrics compared to the traditional uniform gate oxide TFET.

1. Introduction

Recently, scaling of conventional MOSFETs nearly comes to its limit due to complications encountering power consumption as a result of high leakage and excessive dynamic current. MOSFETs approaching the 60 mV/dec subthreshold swing (SS) limit are already in the market, leading to intensified research for what is referred to as *steep slope* switches with SS < 60 mV/dec. One of these proposed switches is the Tunnel FET (TFET) [1]. TFET is of particular significance thanks to its promising advantages, including a lower subthreshold swing (SS < 60 mV/dec) and more efficient operation as a low-power device [2]. In essence, the TFET structure resembles a basic p-i-n diode configuration with a reverse bias applied to a gate-source contact. TFET operation relies on the concept of band-to-band tunneling (BTBT), where charges tunnel from a band on the source side to the other band in the channel side. Afterward, charge carriers are collected by the drain potential [3]. Although TFET appears to be the most promising candidate for mitigating the drawbacks of CMOS caused by extensive downscaling, TFET suffers from a low current handling capability due to its limited BTBT rate. This limitation poses challenges, particularly in Analog/RF circuits [4].

To overcome TFET current limitations, numerous studies of novel structures have been reported. Raising current handling capability can be achieved through the utilization of a dual-gate structure [5]. Further enhancement can be obtained by employing two or three gate materials of distinct metal work functions leading to boosted electrostatic control, a greater tunneling probability, and higher I_{ON}/I_{OFF} [6]. Novel device structures with different channel shapes were presented in the literature.

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Table 1
A summary of the models used and their description.

Model	Description
Non-local BTBT	Tunneling model considering spatial variation of energy bands when non-uniform field dominates
Lombardi	Mobility model, for transverse field dependence
Bandgap Narrowing	Takes the shrinkage of the bandgap into account due to high doping effect
Shockley Read Hall	A recombination mechanism to characterize the statistical behavior of hole and electron recombination, primarily attributed to the trapping mechanism.
Auger	Recombination mechanism accounting for high level injection effects

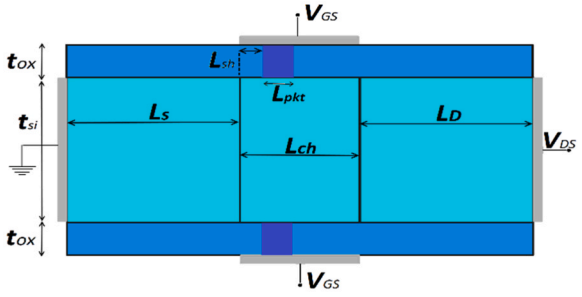

Fig. 1. HDTFET device structure illustrating the major device and biasing factors.

Wang et al. introduced U-shape channel TFET (UTFET), showing an enhancement over planar TFET [7]. Further, L-shaped channel TFET was also discussed in many publications. In [8], the authors discussed guidelines for design of L-shaped channel TFET, while in [9,10], some optimization techniques were applied to boost its performance. UTFET and L-shaped channel TFET were combined in the L-shaped gate TFET, as suggested by [11]. Alternatively, two gates can be used instead of one gate, as proposed by [12], resulting in the T-shaped channel TFET [13]. Gate-all-around TFET was also proposed in [14]. Regarding the source material engineering, SiGe, and semiconducting silicide were introduced in the source region of TFET to form a hetero-junction resulting in improving the device performance, especially the ON current [15–17].

The Hetero-Dielectric TFET (HDTFET) has been proposed and investigated as another potential solution. HDTFET uses an oxide pocket of high-k dielectric near the source region while keeping a low-k dielectric region over the other parts of the device. A high-k dielectric material near the source enhances the ON current. On the other hand, maintaining a low-k material at the drain overcomes the ambipolar current [18,19]. Increasing the high-K region length was found to escalate the gate capacitance reducing circuit bandwidth and lowering speed for the same power as mentioned in [20] and this influence was tested through the investigation of RF performance [21]. Furthermore, some reports shed light on the spacers' dielectric effect on HDTFET performance; [22] proves that using inner high-K and outer low-K spacers, referred to dual-K spacers, improve ON-current and sub-threshold slope. Moreover, charge-based capacitance models of the HDTFET were provided in Ref. [23,24] using an analytical surface potential approach. In addition, instead of inserting high-K dielectric beside low-k dielectric, some research studies considered stack dielectrics over each other [25]. The high-K pocket position was found to influence the DC and analog performance, and an optimum position was suggested in Ref. [17] considering only a single pocket size. In prior investigations, optimization efforts have typically focused on either the ON-state current or cutoff frequency. This study presents a comprehensive approach by conducting a full examination of all relevant parameters, encompassing DC, analog, and digital performance metrics simultaneously.

In this simulation work, we introduce an optimized hetero-dielectric TFET (HDTFET) that integrates a high-k (HfO_2) pocket and low-k (SiO_2) as gate dielectric materials. The placement of the high-k pocket near the source is aimed at controlling tunneling through the source-channel junction. Our study thoroughly investigates the impact of varying the length and position of the HfO_2 pocket along the tunneling interface on

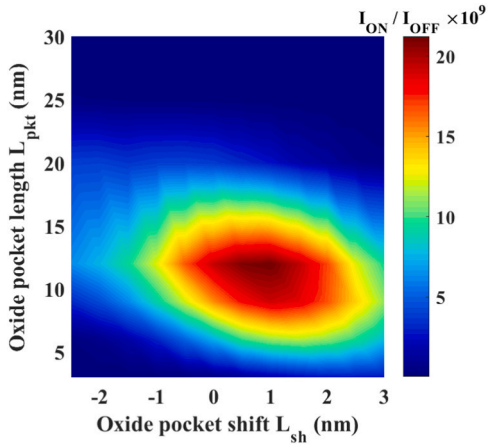

Fig. 3. I_{ON} / I_{OFF} versus pocket size and shift L_{pkt} and L_{Sh}.

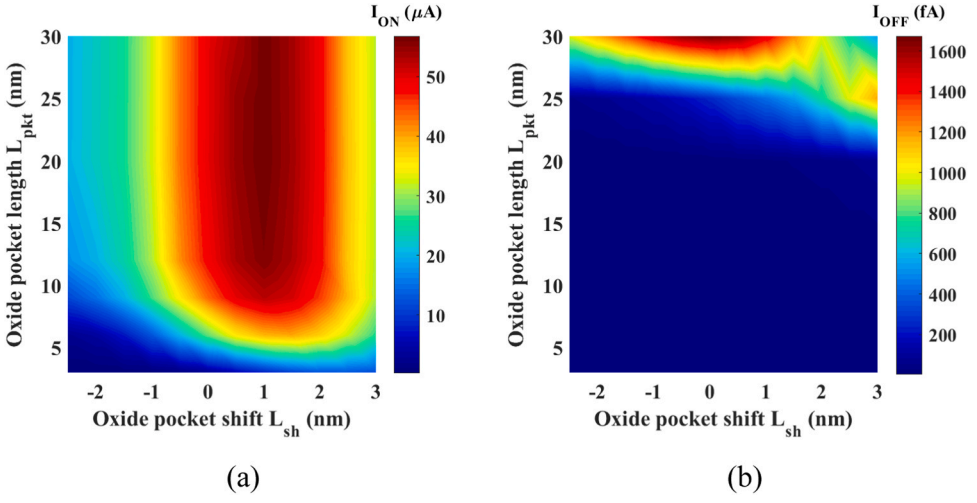

Fig. 2. (a) I_{ON} versus pocket size and shift L_{pkt} and L_{Sh}, (b) I_{OFF} versus pocket size and shift L_{pkt} and L_{Sh}.

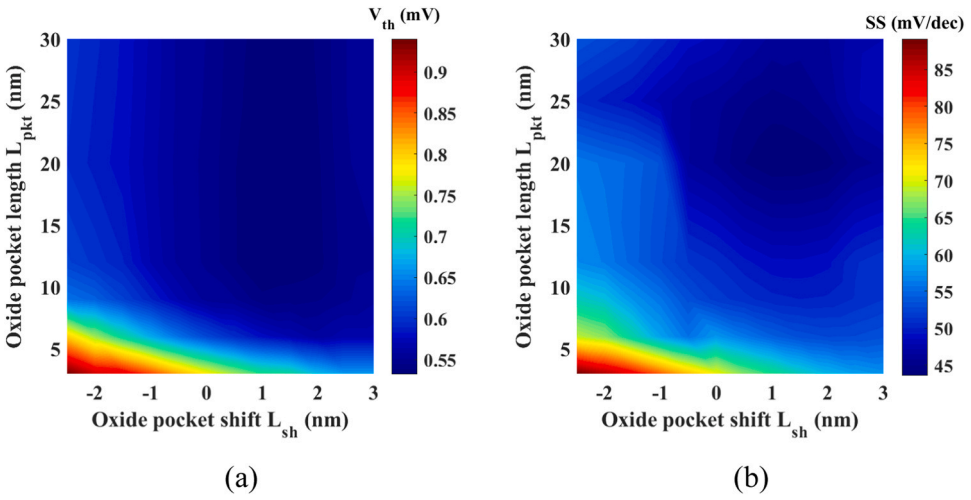

Fig. 4. (a) V_{th} versus pocket size and shift L_{pkt} and L_{Sh}, (b) SS versus pocket size and shift L_{pkt} and L_{Sh}.

DC, analog, and digital circuit-level performance. To comprehensively optimize the pocket parameters, the optimum points are systematically observed within specific ranges: the high-k pocket is shifted across the source-channel junction region, ranging from − 2.5 nm to + 3 nm relative to the junction interface. Simultaneously, at each shift position, the range of the pocket length extends from 10% of the channel length to a maximum of 100% of the channel length (in this case, the pocket covers the entire channel). Beyond and below these selected ranges, there is a deterioration in device parameters, as will be illustrated hereafter. Furthermore, this study demonstrates the scalability for an optimal design with respect to channel length, exploring both upscaling and downscaling. The performance of the device is assessed according to the DC, analog, and transient figures of merit which are determined by ON-state current, I_{ON}/I_{OFF}, and *SS* (DC), cutoff frequency (f_T) (analog) as well as overshoot voltage (V_p) and fall propagation delay (t_{phl}) (transient), respectively.

2. TCAD simulation methodology

The fast evolution of IC technology has driven an urgent need to investigate diverse devices and simplify fabrication processes, underscoring the immense value of TCAD simulations. By applying TCAD models, novel device designs can be examined to enhance the performance of present or developed devices. It has been comprehensively validated that TCAD simulators are effective and economical tools to investigate and test novel devices like TFETs [17,26].

All simulation studies performed in our presented work have been accomplished employing Atlas device simulator within Silvaco framework. ATLAS provides general capabilities for numerical, physics-based simulation for the device under investigation. It estimates the electrical characteristics of various device configurations and offers insights into their underlying physical mechanisms. The outcomes of the simulation depend on the device material parameters and the models used. Thus, it is crucial that the various parameters are known to the best accuracy and the material models are chosen correctly. The right choice of models requires a good understanding of the device behavior, and a proper parameter selection depends on how well a material system has been studied.

The following physical models are used during the simulations. To evaluate the tunneling generation rates throughout the device structure, the non-local band-to-band-tunneling (BTBT) model was exploited. To obtain reliable accuracy, fine meshing in space as well as quantum tunneling meshing are specified. The mobility model invoked in simulation is Lombardi model which considers the influences of temperature, doping density, and both lateral and perpendicular electric fields. The band gap narrowing model was also allowed to take high doping effects into consideration [27]. The recombination models such as Shockley Read Hall, and Auger mechanisms are enabled. Finally, the main DC and small signal parameters are extracted where the small-signal AC analysis is carried out at frequency of 1 MHz. Before performing the optimization of the presented device structure, firstly, relative electron and hole effective masses were selected as 0.12 and 0.17, respectively [28]. The criterion of choosing these values is based on the calibration for a conventional silicon TFET against published work that was previously calibrated with measurements of tunnel diodes from IBM [5]. A summary of the models used and their significance is represented in Table 1 [27].

3. Device configuration and parameters

A cross-sectional interpretation of HDTFET that invokes the pocket of HfO_2 (of variable length and position) and SiO_2 as gate oxide materials is illustrated in Fig. 1. The main device factors utilized in TCAD simulations are as follows (based on previous work [17,29]). The length of the source (L_s) and drain (L_d) is 50 nm, meanwhile, the channel length (L_{ch}) is chosen to be 30 nm. The gate dielectric thickness (t_{ox}) is set at 3 nm, while the Si film thickness (t_{Si}) is taken to be 10 nm. The source (N_s), channel (N_{ch}) and drain doping (N_d) concentrations are taken to be 1×10^{20} cm^{-3} (p-type), 1×10^{17} cm^{-3} (n-type), and 5×10^{18} cm^{-3} (n-type), respectively. The gate contact work function is fixed at 4.5 eV, which is suitable for polysilicon, Titanium, and Tungsten as gate materials. The leakage tunneling current through the gate oxide is neglected as the effective oxide thickness is within the accepted range for avoiding such current [30,31].

In our analysis, the static figures of merit are: the ON-state current (I_{ON}) computed at $V_{GS} = 1$ V and $V_{DS} = 1$ V, OFF-state current (I_{OFF}) evaluated at $V_{GS} = 0$ V and $V_{DS} = 1$ V, and *SS* calculated from the change in V_{GS} that should be utilized to produce a one decade rise in drain current [29]. Considering the dynamic performance, f_T is taken as a figure of merit. The cutoff frequency can be extracted from, $f_T = g_m/2\pi C_{gg}$, where g_m is the transconductance and C_{gg} is the overall capacitance calculated as, $C_{gg} = C_{gs} + C_{gd}$, where C_{gs} is the gate-source capacitance, while C_{gd} is the gate-drain capacitance.

4. Results and discussion

In the subsequent simulations, the high-k pocket length is systematically altered as well as its position relative to the source-channel interface. Firstly, the impact of this double sweep on the DC parameters (I_{ON}, I_{OFF}, ON/OFF ratio, threshold voltage and *SS*) is investigated.

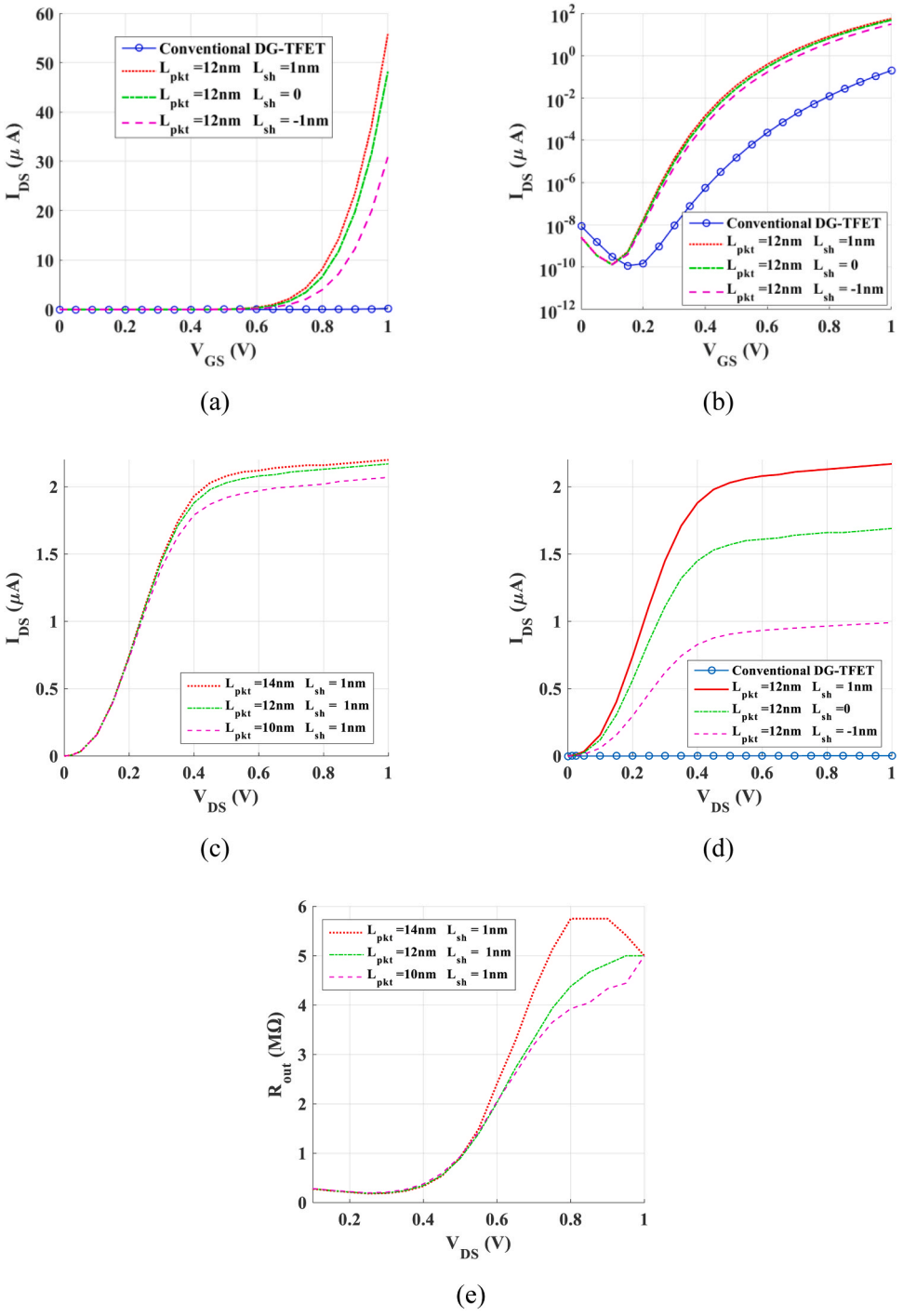

Fig. 5. Drain current vs gate voltage (a) linear scale and (b) semi log scale, (c) drain current vs gate current with different pocket sizes at a fixed pocket shift of 1 nm, (d) pocket shift at a fixed pocket length of 12 nm, and (e) output resistance vs drain-source voltage for different pocket dimension.

Next, the impact on the analog/RF parameters is explored. The optimization of the length and shift of the pocket is done to search for the possible maximum ON/OFF ratio, maximum cutoff frequency and minimum SS. The incorporation of the TFET structure in an inverter circuit is investigated and some design guidelines are provided. Finally, we investigate the influence of the channel scaling.

4.1. Impact of pocket parameters on DC performance

The ON current variation is represented at different shift values (L_{Sh}) and different high-k pocket length (L_{pkt}) as displayed in Fig. 2a. The range in which L_{Sh} and L_{pkt} varies is from − 2.5 nm to 3 nm and from 0 to 30 nm, respectively. As clearly seen in the figure, there is an optimum value for pocket shift around 0.5 nm away from source side. On the other hand, the pocket size has no absolute maximum. As the pocket size increases from 2.5 nm to 10 nm, the ON-state current increases drastically; however, further increase in pocket size causes slight increase in I_{ON} then the current saturates. Interestingly, only one-third of channel length needs a cover of high-k oxide to get the maximum current. This portion is enough to directly modulate tunneling width at the source side [32]. Further increase in pocket size than one-third of channel length increases gate capacitance as will be presented later. Accordingly,

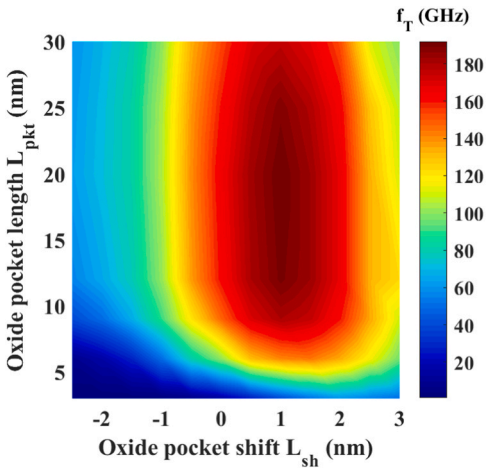

Fig. 6. f_T versus pocket size and shift L_{pkt} and L_{Sh}.

keeping pocket length around one-third appears to be an optimal point for both current and capacitance in this design.

Fig. 2b depicts I_{OFF} for different pocket sizes and positions. For a small pocket size, it has negligible effect on the OFF-state current wherever the pocket position is. As the size increases, the high-k region becomes closer to the drain side. Hence, the drain voltage can affect the channel region, causing the current to increase rapidly for negative and small positive pocket shifts. As the pocket shifts further towards the drain and moves away from the source, the effect of drain voltage on the channel region decreases slightly, causing a reduction in current. In other words, the impact of the pocket shift on I_{OFF} is negligible, whereas the pocket length leads to an increase in the OFF current. Since studying the OFF-state current alone here is tricky to judge its performance and needs extra accuracy, it is better to check the ratio of ON-state current to OFF-state current which is depicted in Fig. 3. Vividly, I_{ON}/I_{OFF} has a peak at pocket shift and length of 1 nm and 12 nm, respectively. These values are near to the optimum values reported by optimizing ON-state current alone.

Moreover, the threshold voltage is depicted in Fig. 4a. From pocket size viewpoint, as pocket size increases, the high-k oxide facilitates the gate functioning to control the channel and tunnel regions causing V_{th} to drop accordingly. Meanwhile, for the same pocket size, the threshold voltage increases as pocket moves toward source side. This effect is more pronounced for small pocket sizes. The optimum proposed point has a threshold voltage of 550 mV, which is close to the minimum value. For a 1 V supply voltage, this value (almost half the supply voltage) is attractive for digital CMOS circuits to reduce current spikes during switching. However, for analog circuits, this value is a little high and can be reduced by increasing permittivity of gate oxide or decreasing gate oxide thickness, beside controlling gate metal stack.

Next, Fig. 4b shows the subthreshold swing variation according to the variation of pocket shift and size. Apparently, *SS* has the same trend as V_{th}. Comparing to the 60 mV/dec of ideal conventional MOSFET, HDTFET can achieve *SS* of 45 mV/dec for a pocket width and a shift of 22 nm and 1.5 nm, respectively. An *SS* of nearly 55 mV/dec is achieved

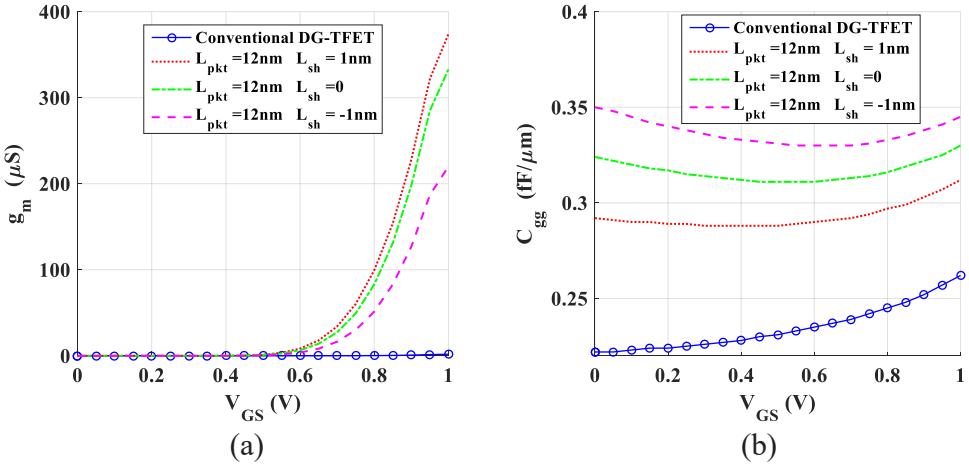

Fig. 7. (a) Transconductance vs gate voltage, (b) Gate capacitance vs gate voltage.

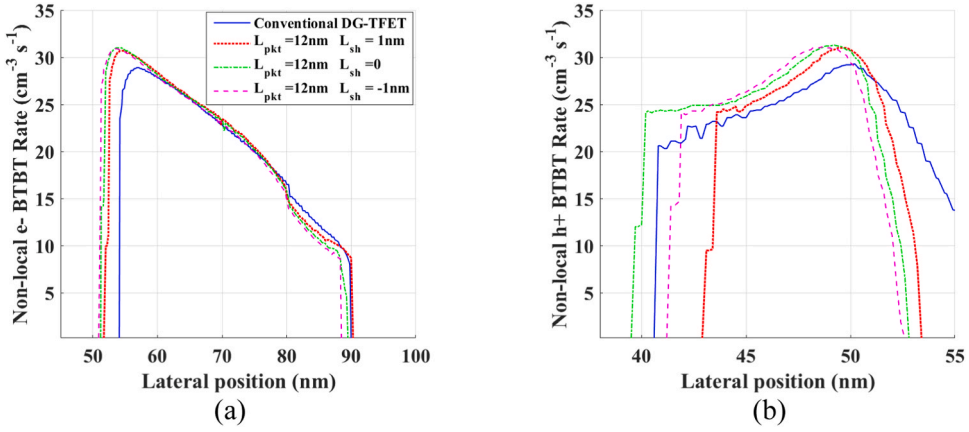

Fig. 8. (a) non-local electron BTB tunneling rate, (b) non-local hole BTB tunneling rate.

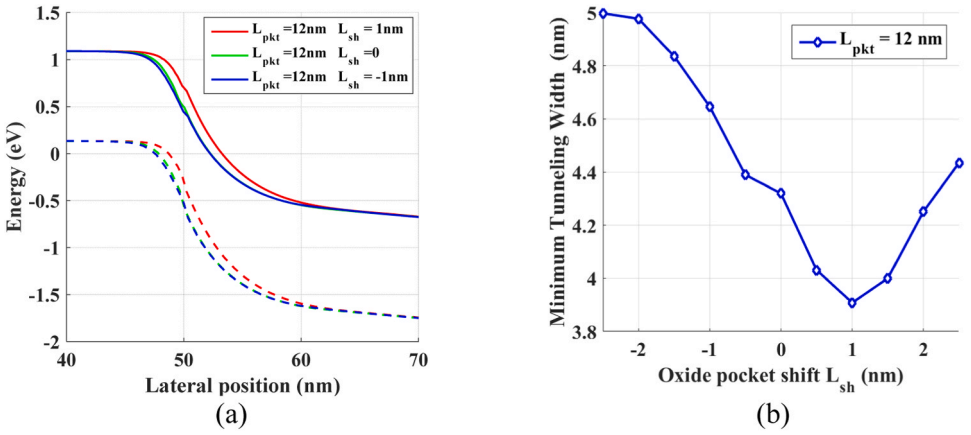

Fig. 9. (a) Energy band diagram and minimum tunneling width for different pocket shifts.

Table 2
Summary of optimization range of each parameter and optimum values achieved.

Parameter	Optimum value	Corresponding L_{sh}	Corresponding L_{pkt}	Value of optimum design L_{Sh} = 1 nm, L_{pkt} = 12 nm	Conventional DG-TFET
I_{ON}	55 μA/μm	0.5: 1.5 nm	10: 30 nm	54 μA/μm	0.2 μA/μm
I_{ON} /I_{OFF}	20 × 10^9 A/A	-1: 2 nm	7: 15 nm	20 × 10^9 A/A	2 × 10^7 A/A
V_{th}	550 mV	0.5: 2 nm	10: 30 nm	550 mV	942 mV
SS	45 mV/dec	0.5: 2 nm	18: 25 nm	55 mV/dec	89 mV/dec
f_T	194 GHz	0.5: 1.5 nm	8: 25 nm	190 GHz	1.1 GHz

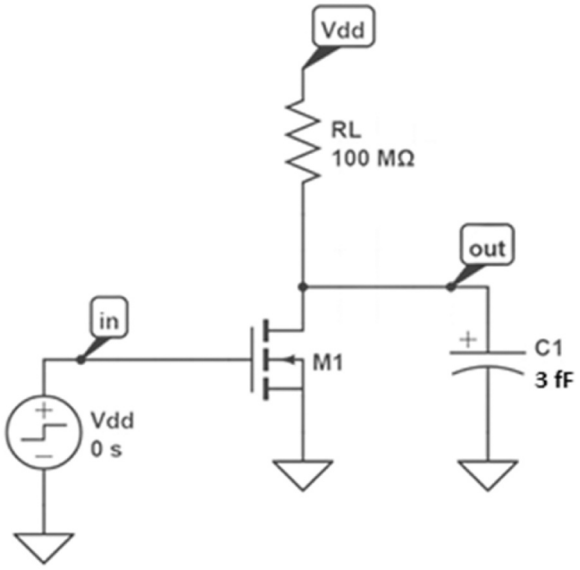

Fig. 10. Resistive based inverter circuit.

for the optimum- I_{ON}/I_{OFF} point (L_{Sh} and L_{pkt} is 1 nm and 12 nm). It can be inferred that the pocket size required to achieve better *SS* decreases for higher positive values of L_{Sh}. Based on the previous DC simulations, the optimum choice for L_{Sh} and L_{pkt} is 1 nm and 12 nm, respectively. These values maximize both ON-state current and V_{th} without a significant loss in SS.

It is clear from Fig. 2a, that at a pocket length of 12 nm, the ON-current starts to saturate. Accordingly, we will proceed with this length in the following analysis. The I-V transfer characteristics of length 12 nm are illustrated in Fig. 5a and b, represented by linear and semi-log scales, respectively. Compared to the simulated conventional DG-TFET current with the same dimensions, as shown in the figure, inserting a High-K pocket boosts the ON-state current by more than an order of magnitude. The output characteristics with different pocket thicknesses and positions are illustrated in Fig. 5c and d, respectively for V_{GS} of 0.7 V. For the same shift and different pocket thickness, a slight difference is shown in current saturation with nearly the same output impedance (roughly 5 MΩ). On the other side, keeping the same pocket size while shifting the pocket size to positive direction lowers output impedance in linear region; however, manifests the same 5 MΩ in saturation region, and pushes the saturation voltage to higher value (see Fig. 5e).

4.2. *Impact of pocket parameters on analog performance*

The variation of the cutoff frequency (which is a measure of the device speed) is presented in Fig. 6 at V_{GS} and V_{DS} of 1 V. Like the trend of I_{ON}, f_T increases drastically with pocket size for small size values. In addition, an optimum point can be considered at pocket shift and width of 1 nm and 12 nm, respectively, which is the same as reported from the trend of I_{ON}/I_{OFF}. For a small pocket size less than 12 nm, f_T is dominated by g_m (which is proportional to I_{ON} and shown in Fig. 7.a) following the same attitude of I_{ON}. At a larger pocket size, C_{gg} dominates the f_T trend, causing f_T to decrease due to the increase in the capacitance. The rise of C_{gg}, in Fig. 7.b, can be explained by Miller effect. As the size of the high-k pocket increases, the gate exhibits higher capacitance, signifying an increase in C_{gd}, which results in a reduction of f_T. To mitigate this Miller effect and prevent a reduction in f_T, it is advisable to avoid placing the high-k oxide near the drain side.

An optimum range of pocket size is proposed: L_{pkt} ranges from 10 nm to 20 nm (40% of channel length) can effectively prevent Miller effect (see Fig. 6), with the pocket shift maintained at 1 nm.

The electron and hole tunneling rates are illustrated in Fig. 8.a and Fig. 8.b, respectively. It is clear that tunneling peaks occur at a lateral position of 50 nm at which the gate potential has the greatest modulation effect on tunneling width and, consequently, the tunneling rate. Far from this value, the tunneling rate declines as tunneling width increases. Additionally, Fig. 9 displays the minimum tunneling width as a function of the pocket shift (for a pocket length of 12 nm). The simulation results show that a pocket shift of 1 nm provides the minimum tunneling width

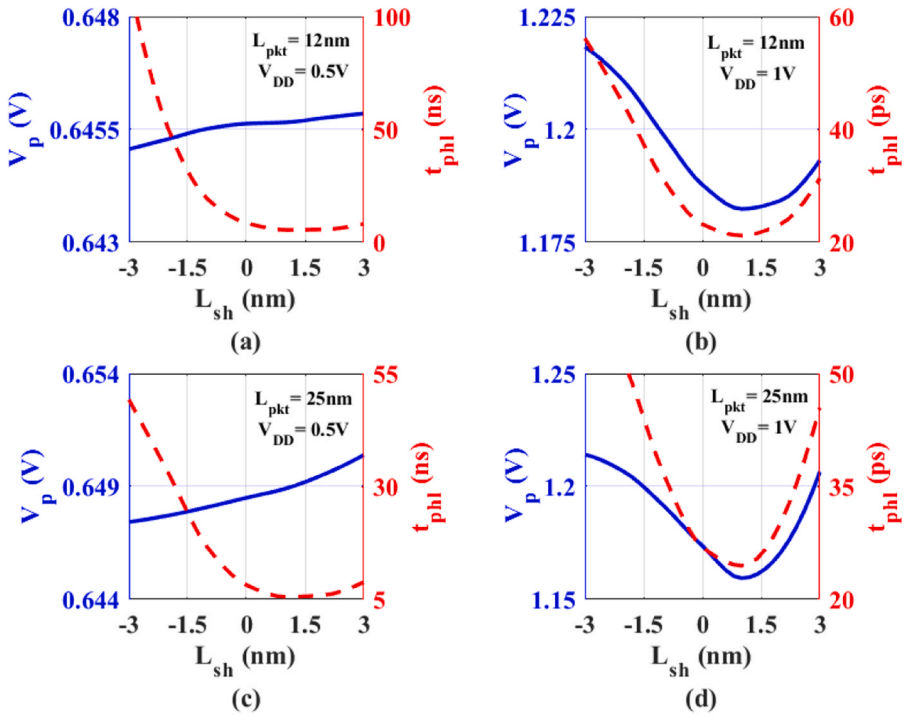

Fig. 11. Overvoltage and high-to-low delay for different values of V_{DD} and L_{pkt}: (a) V_{DD} = 0.5 V and L_{pkt} = 12 nm, (b) V_{DD} = 1 V and L_{pkt} = 25 nm, (c) V_{DD} = 0.5 V and L_{pkt} = 12 nm, and (d) V_{DD} = 1 V and L_{pkt} = 25 nm.

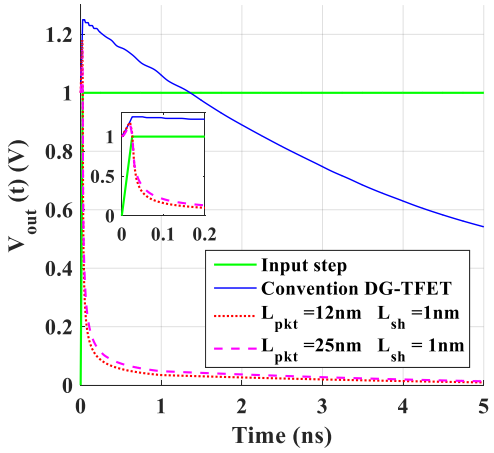

Fig. 12. Comparison of V_{out}(t) for conversional DG-TFET vs proposed design.

as expected.

Table 2 presents a design chart to optimize a specific parameter or a figure of merit. For example, we can choose an optimum point for analog circuit parameters (L_{Sh} =1 nm, L_{pkt} =12 nm) that gives nearly the highest current and cut-off frequency. On the other hand, for digital flavor, we can optimize for SS and V_{th} to reduce leakage current in CMOS circuits. Following the same strategy, this table can be used to determine the optimum design for a certain application.

4.3. Impact of pocket parameters on switching performance

In this subsection, the n-HDTFET is tested in a conventional inverter circuit in which the load is a resistive load (R_L) in parallel to a capacitance (C_L). The circuit is displayed in Fig. 10, where the input voltage is a pulse, whose amplitude is equal to the supply voltage. In order to examine the voltage scaling effect on device performance, supply voltages of 0.5 V and 1 V are used. The rise time is 20 ps, while R_L = 100 MΩ, and C_L = 3 fF. The results of the transient analysis of the presented circuit for various L_{Sh} values are demonstrated in Fig. 11.

The optimum shift with respect to overshooting and delay time varies with pocket shift and width. For a pocket length of 12 nm, the optimum shift of 1 nm is observed for both supply values. However, for a 25 nm length, the optimum is 1 nm for the delay and overshooting when a 1 V supply is utilized. When a supply of 0.5 V is used with a pocket length of 25 nm, the delay has an optimum shift around 1 nm, meanwhile overshoot optimum is not observed. There is no sharp optimum when the supply is less than V_{th} (i.e. for V_{DD} = 0.5 V). However, for higher voltages, there is an optimum, as shown in Fig. 11b and d. Fig. 12 shows input/output waveforms of the two pocket lengths compared to conventional DG-TFET.

4.4. Channel scaling

Based on the analysis of the 30 nm channel TFET structure, it was found that the channel needs insertion of high-K pocket material with 40% length and 2.5% shift with respect to the total channel length in order to optimize different parameters, especially ON/OFF current ratio. In this subsection, we verify the ratios of 40% and 2.5% for different channel length designs, either scaling down or up, by applying the analysis to various HG-TFETs with gate lengths ranging from 20 nm to 50 nm. Fig. 13(a), (b), and (c), showing ON/OFF current ratio for channel lengths of 20, 40, and 50 nm respectively, proves the reported optimum ratios that are listed in Table 3. Moreover, energy band diagrams for the three channel lengths are depicted in Figure 13(d)–(f) for given L_{pkt} and L_{Sh} values.

Finally, the proposed design offers advantages in terms of scalability with channel length and presents a tradeoff between ON-state current and cutoff frequency. A detailed comparison with various TFET architectures is provided in Table 4. In all these device structures, hetero dielectric (HD) oxides are utilized. Notably, most of these studies lack consideration for cutoff frequency, making it challenging to make a fair judgment on each architecture. For instance, in Ref [15], higher current and improved subthreshold swing are reported; however, cutoff

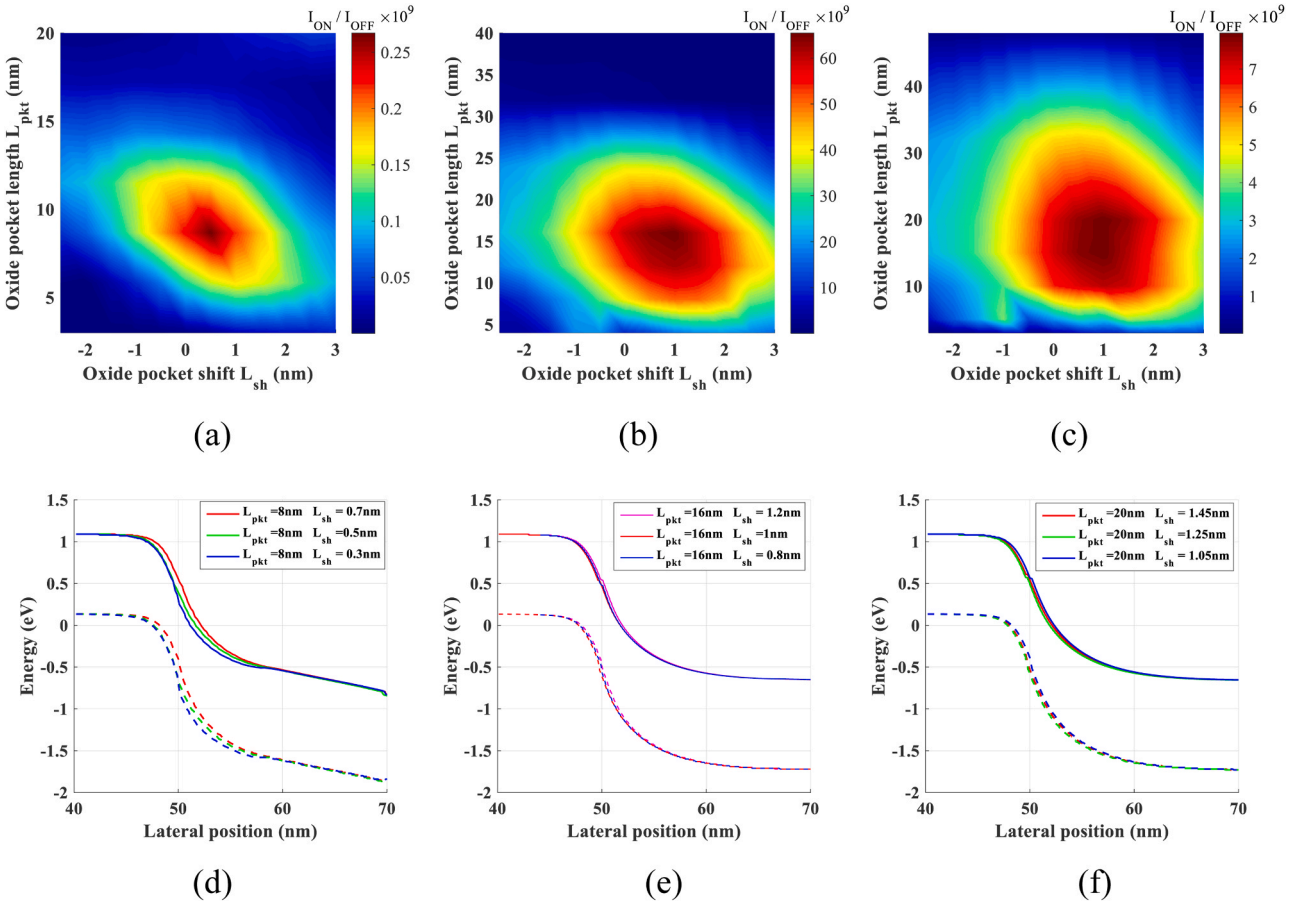

Fig. 13. (a), (b), and (c) I_{ON}/I_{OFF} ratio for channel lengths of 20, 40, and 50 nm respectively, and (d), (e) and (f) corresponding band profiles for given values of L_{pkt} and L_{Sh}.

Table 3
Optimum width for ON/OFF current ratio, current ratio values, and f_T.

Channel Length (nm)	20	30	40	50
Optimum pocket length (nm)	8	12	16	20
Optimum pocket position (nm)	0.5	0.75	1	~1.25
I_{ON}/I_{OFF} ($\times 10^9$)	0.21	21	65	79
f_T (GHz)	100	175	194	191

frequency is not addressed, besides the associated increased cost of SiGe. In all works, the length of the pocket is taken to be fixed. In Ref [29], the pocket shift was varied, resulting in an improvement in device performance. However, regarding our approach, more advancements can be realized as indicated in the table. Upon optimizing the pocket length for a channel length of 50 nm, the ON/OFF current ratio has been increased as indicated.

The miniaturization of integrated circuits (ICs) is a compelling objective, and despite the challenges associated with designing a 30-nm channel length in the context of TFET design, it holds considerable appeal. Notably, the fabrication of the suggested TFET with a high-k pocket of such narrow width and precise alignment introduces a significant challenge, complicating the manufacturing process. Despite these hurdles, the substantial enhancement in overall device characteristics justifies exploring the fabrication of such devices, especially considering recent advancements in nanotechnology.

It should be pointed out here that our proposed design can be applied for other materials like III-V, in which heterostructures can be employed for better control of the tunneling area. Moreover, AI models can be engaged for optimization, offering efficiency in terms of time and area

Table 4
Comparison of achieved parameter values vs previous work.

	Ref. [15]	Ref. [14]	Ref. [16]	Ref. [29]	Our Work	Our Work
Structure	Single-gateHD gate SiGe source	Single-gateHD gate fixed length	Single-gateHD gate SiGe source	Double-gate HD gate fixed length	Double-gateHD gate tunable position and length	Double-gateHD gate tunable position and length
Gate length	50 nm	50 nm	50 nm	50 nm	50 nm	30 nm
t_{ox} (nm)	4 (SiO_2)	2 (SiO_2)	4 (SiO_2)	3 (SiO_2)	3 (SiO_2)	3 (SiO_2)
Pocket	20 nm-HfO_2	6 nm-HfO_2	20 nm-HfO_2	5 nm-HfO_2	20 nm-HfO_2	12 nm-HfO_2
V_{DD} (V)	2.5	1	1.2	1	1	1
I_{ON} (μA/μm)	1.2e3 (V_G = 2.5 V)	27 (V_D= 0.5 V)	1.43 (V_G = 1.2 V)	54 (V_G = 1 V, 1 nm-Shift)	59 (V_G = 1 V, 1 nm-Shift)	55 (V_G = 1 V, 1 nm-Shift)
I_{ON}/I_{OFF}	100e9	370e6	500e6	70e9	79e9	20e9
SS (mV/dec)	40.4	~56	45	42	42.5	55
f_T (GHz)	–	–	–	185	191	175

during extensive parameter sweeps [33–36].

5. Conclusion

In this work, TCAD numerical simulator was utilized to optimize the position shift and size of a high-k pocket in HDTFET on the device parameters for DC, analog and digital performance. Through our analysis, we identified an optimal shift and width of approximately 1 nm and 12 nm, respectively, for a 30 nm-channel length. The optimized design maximizes the ON-state current, and speed reflected in f_T. Considering those optimum values for a 30 nm-channel, the design accomplished an ON-state current of 54 μA/μm, I_{ON}/I_{OFF} of 20×10^9, SS of 55 mV/decade, and a maximum f_T of 175 GHz. Furthermore, when integrated into a resistive load inverter circuit, the optimized TFET structure exhibited a fall time of 20 ps when supplied by 1 V. Supply scaling down remarkably slows down the transient behavior. Further, reducing the supply by half resulted in a justified decrease in fall time to 15 ns, attributed to the diminished sub-threshold current.

Additionally, optimum design scalability with channel length were proven to be 40% for pocket size and around 2.5% for pocket shift.

These optimized characteristics prove adaptable structure for both analog and digital systems. Fine-tuning around these values can be explored to tailor performance for specific applications. These results highlight the promising performance potential of our design guidelines. As part of future work, we aim to extend the applicability of the proposed optimization strategy beyond silicon to III-V compound semiconductors. Additionally, exploring the potential of stacked gate oxide configurations, as opposed to a single-layer oxide, represents a promising avenue for further research.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper. No financial interests/personal relationships.

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