




## Article

# Performance Improvement of npn Solar Cell Microstructure by TCAD Simulation: Role of Emitter Contact and ARC

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**Abstract:** In the current study, the performance of the npn solar cell (SC) microstructure is improved by inspecting some modifications to provide possible paths for fabrication techniques of the structure. The npn microstructure is simulated by applying a process simulator by starting with a heavily doped *p*-type substrate which could be based on low-cost Si wafers. After etching deep notches through the substrate and forming the emitter by *n*-type diffusion, an aluminum layer is deposited to form the emitter electrode with about 0.1  $\mu\text{m}$  thickness; thereby, the notches are partially filled. This nearly-open-notches microstructure, using thin metal instead of filling the notch completely with Al, gives an efficiency of 15.3%, which is higher than the conventional structure by 0.8%. Moreover, as antireflection coating (ARC) techniques play a crucial role in decreasing the front surface reflectivity, we apply different ARC schemes to inspect their influence on the optical performance. The influence of utilizing single layer (ZnO), double ( $\text{Si}_3\text{N}_4/\text{ZnO}$ ), and triple ( $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{ZnO}$ ) ARC systems is investigated, and the simulation results are compared. The improvement in the structure performance because of the inclusion of ARC is evaluated by the relative change in the efficiency ( $\Delta\eta$ ). In the single, double, and triple ARC,  $\Delta\eta$  is found to be 12.5%, 15.4%, and 17%, respectively. All simulations are performed by using a full TCAD process and device simulators under AM1.5 illumination.

**Keywords:** npn microstructure; heavily doped wafers; low cost; emitter contact; ARC; TCAD



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## 1. Introduction

Recently, the photovoltaic (PV) technology has been widely investigated as a favorable renewable clean energy resource to solve the concerns related to global energy [1]. The contribution of installed PVs to global electricity needs attained more than 750 GW in 2020 with a predicted growth to more than 1200 GW by 2024 [2–4]. In this context, solar cells (SCs) are being developed to enhance solar power generation efficiency [5]. A lot of emerging materials have been established to be utilized in thin-film SCs. These materials demonstrate increasing efficiencies, for instance, up to 25.6% for perovskite, 23.4% for CIGS, 21.0% for CdTe, and 19% for organic, and 15.3% for polymer SCs [2,6–12]. However, thin film technologies are typically more expensive than silicon-based SCs for mass applications.

Remarkably, crystalline silicon (c-Si) SCs are considered the most dominant cells encountered in PV technology as they share over 90% of the global solar market [13]. Efficiencies of more than 26% for the c-Si SCs have been reported [14], while the theoretical

PCE is about 32.7% on the grounds of the Shockley–Queisser limit for the c-Si  $p$ - $n$  junction SC [15]. Different efforts were devoted to producing high-efficiency c-Si SCs, including laser-doped selective emitters (LDSE) [16], passivated emitter and rear cell (PERC) [17], interdigitated back cell (IBC) [18], and other configurations [19]. Although some structures, whose operation is based on the  $p$ - $n$  homojunction confronted in c-Si SCs, were investigated [20–24], the unsatisfactory efficiency or the toxicity issues of these cells may limit their commercialization. So, it is expected that Si-based SCs will still lead the market for at least the coming years. Apart from the efficiency issue, another important factor is to decrease cell manufacturing costs. Silicon wafers and silver paste are the main factors that increase the cost during SC manufacturing [5]. Thus, it is crucial to find out ways of reducing the SC cost, and thereby the overall PV cost, by engineering the Si wafers and silver paste.

In the conventional c-Si SCs, when photons are absorbed by silicon, electron-hole pairs are produced, and the collection of these carriers is in the same path as the absorption. This process requires a thick Si-wafer, in the order of 300  $\mu\text{m}$ , as the absorption coefficient of Si is relatively low. Thus, lightly doped wafers are required to achieve desirable long minority diffusion lengths in the order of the large thickness of the wafer [25]. The lightly doped wafers need zone refining processing steps, which increase the cost of the cell and thereby the overall cost of the PV module. An approach to prevent the need for high diffusion lengths (thus high-quality high-cost Si wafers) is to employ a device structure that satisfies the uncoupling paths of light absorption and carrier collection [26–28]. This is the idea of our presented microstructure in which the SC is relatively thick in the path of incident radiation to expand the absorption of photons, but quite thin in the carrier collection direction to assist in the effective collection of photogenerated charge carriers [25]. Thus, the width of the microstructure can be tweaked to be less than or equal to the diffusion length in order to ensure that photoexcited charge carriers are collected before recombination happens. Besides, the thickness of the solar cell can be adjusted to keep the photon absorption as maximum as possible while reducing the cost. Regarding experimental efforts, it was reported that an efficiency of 7.8% was achieved for Si micro-gratings having vertical sidewall electrodes [29]. Further, a high-performance micro-pillar Si SC structure having Cu nanoparticles was synthesized, and an efficiency of 11.5% was reported [30]. Such ideas, both theoretically and experimentally, can open a path for utilizing Si wafers with heavy doping, which are distinguished by their low processing cost, for SC fabrication [31,32]. Recently, an npn microstructure has been suggested, which is based on a high-doped Si wafer as a  $p$ -type substrate. The efficiency of the proposed test structure recorded an initial value of 10.7% based on TCAD simulations [33]. After the optimization of its key design factors, it achieved about 14.5% efficiency [34,35]. In this structure, the produced notches by a process simulator were filled completely by Al which may limit the efficiency due to higher optical losses.

The main factors that cause the efficiency degradation of a SC are categorized as recombination, resistance, and optical losses. To control the recombination loss on the back or the upper SC surface, a back surface field (BSF) layer with high doping or a passivation layer is applied, respectively. The resistance losses, either series or shunt, can be reduced through the proper design of the metal bars. The optical losses result from either the front electrode, which cause shadowing effect, or reflections from the SC surface [36]. To decrease the optical losses due to the front electrode, open notches are more significant than closed ones to achieve photon absorption all over the whole surface of the cell. Further, it has been reported both theoretically and experimentally that the energy loss because of reflection can be relieved through the deposition of antireflection coating (ARC) layers on Si [37]. In this regard, many research studies have been reported to investigate single, double, and multilayer antireflection coatings utilizing various kinds of materials, such as  $\text{TiO}_2$  and  $\text{Si}_3\text{N}_4$  [38],  $\text{SiO}_2/\text{Si}_3\text{N}_4$ ,  $\text{SiO}_2/\text{TiO}_2$ ,  $\text{ZnS}/\text{MgF}_2$ , and  $\text{SiN}_x\text{:H}/\text{SiO}_x\text{N}_y/\text{SiO}_x$  [39–41].

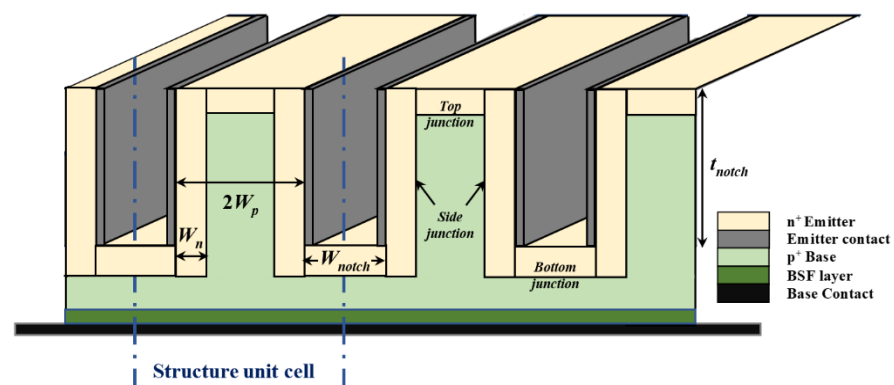
Moreover, plasmonic nanostructures have been recently studied as a potential approach for enhancing light absorption in SCs [42,43]. The powerful interaction of small

metal nanostructures with light permits control over light propagation; thereby, light can be trapped in the photoactive region and can be effectively absorbed. It was reported that a layer of Ag nanoparticles can boost the standard ARC employed in SCs [44,45]. Additionally, metal gratings have been utilized for light trapping. The influence of a periodic array of Ag strips on the absorption behavior of Si SCs has been numerically studied showing an enhancement of more than 50% in photocurrent [46]. However, the deposition of metallic nanoparticles atop c-Si SCs involves additional covering layers being applied, which raises the overall production cost [2,42].

As mentioned herein, the two main areas of interest to accomplish an efficient PV system are the cost and the efficiency of the solar cells. In the current work, we present a simulation study of a proposed structure where we try to combine lower cost with higher efficiency. The structure can be established by employing a high doping level *p*-type wafer whose thickness may be less than 100  $\mu\text{m}$ . Furthermore, the structure design is based on reducing the shadowing effect by incorporating open notches. Additionally, the ARC can be used to decrease the optical losses due to surface reflections. Thus, the factors that adversely affect efficiency can be alleviated by the proposed ideas. Before the actual fabrication of our microstructure, process and device simulations are mandatory to define and fine-tune the design parameters and to precisely predict the device performance. Therefore, we also provide a proposed process flow here to guide the fabrication of this promising npn SC microstructure.

## 2. Materials and Methods

Figure 1 displays a 3D view of the partially-filled-notches npn SC microstructure. The primary purpose of this configuration is to remove the metal from the structure notches, unlike the conventional structure in which the notches are completely filled with metal [31–35]. Therefore, this modified structure has the advantage of reducing the shadowing effect, thus activating the bottom planar solar cell, which will contribute to enhancing the structure performance. Consequently, it is qualitatively expected that both the optical and electrical performance of the presented SC structure will be better than the conventional fully filled notches structure. The different *p*-*n* junctions involved in the cell are divided into the top, bottom, and side junctions. The main junctions which contribute to photon collection are the side ones; however, the top junction has a useful function of capturing the ultraviolet part of solar radiation [33], while the bottom junction enhances the short circuit current, as will be demonstrated hereafter.

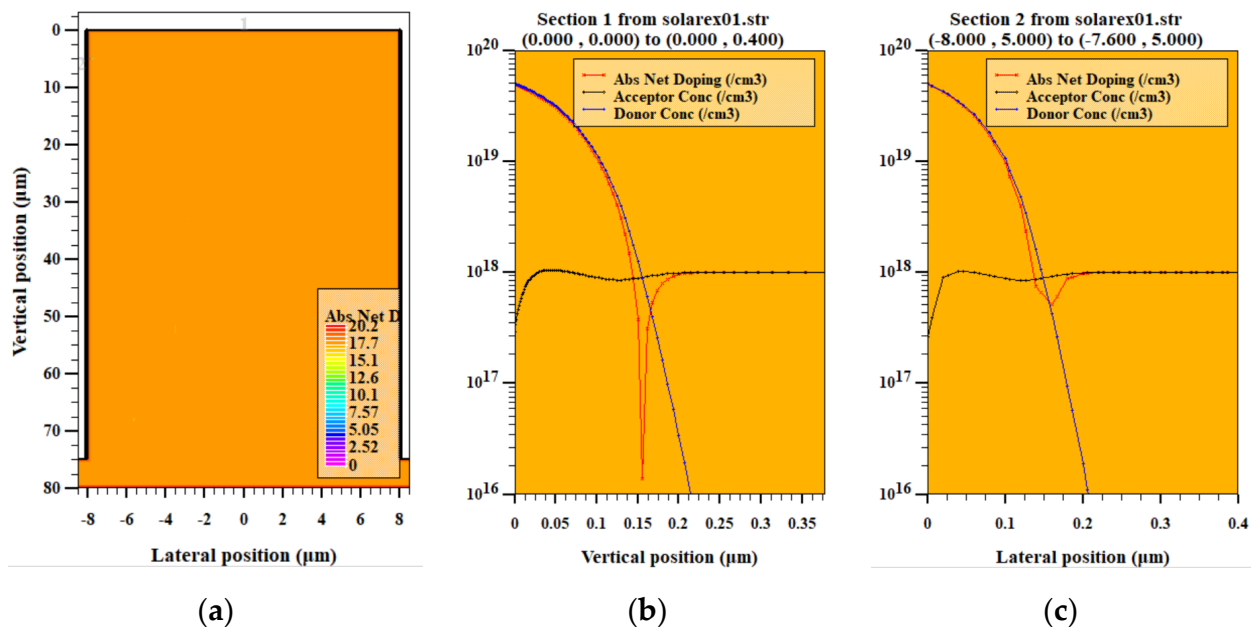


**Figure 1.** 3D schematic representation of the partially-filled-notches npn solar cell microstructure utilized in the study.

The partially filled notches npn microstructure has the same technological and physical parameters as the conventional one considered in our previous work [34,35], except that the nearly open notches have a thin aluminum 0.1  $\mu\text{m}$  film on the structure sidewalls, as is depicted in Figure 1. This metal layer serves as the cathode electrode of the structure. The key parameters of the structure are listed as follows (see Figure 1). The  $p^+$  base width

is  $2W_p$ , where  $W_p$  is the width of the base region that is set to  $W_p = 8 \mu\text{m}$ . The  $n^+$  layer thickness can be tuned according to the diffusion process via a process simulator. For our structure, it is found from our previous work that a width of the  $n^+$  side wall emitter ( $W_n$ ) of about  $0.18 \mu\text{m}$  gives an optimum efficiency. The thickness of the thin wafer is taken to be  $80 \mu\text{m}$ . This thickness is beneficial for lowering the cost and it is actually a demand for future wafers to be less than  $100 \mu\text{m}$ , as the cost of wafers is considered the most severe factor that results in increasing the PV module cost. The doping densities of the  $p^+$ -base,  $n^+$ -side emitter are  $N_{p+,base} = 10^{18} \text{cm}^{-3}$  and  $N_{n+,emitter} = 5 \times 10^{19} \text{cm}^{-3}$ . Regarding the notch width and thickness, they are taken as  $W_{notch} = 2 \mu\text{m}$  and  $t_{notch} = 75 \mu\text{m}$ . The reasons behind choosing such design values were thoroughly discussed and claimed in our previous work [31–35].

The simulation of the proposed solar cell is executed by exploiting the SILVACO TCAD process and device simulators, following the subsequent steps. First, the microstructure SC is realized by using a SILVACO process simulator (Athena) [47]. In the Athena process simulator, after defining the mesh, a Si wafer that acts as a substrate is defined. The doping of the substrate is  $p$ -type boron with a concentration of  $1 \times 10^{18} \text{cm}^{-3}$ , while the wafer orientation is chosen to be (100). The grooves are then defined by an etching process producing open trenches that are  $2 \mu\text{m}$  in width and  $75 \mu\text{m}$  in depth. The  $n^+$  emitter is produced by the diffusion of phosphorous to obtain a concentration of about  $5 \times 10^{19} \text{cm}^{-3}$ . Next, the sidewall electrodes are formed, and the metal is etched from the surfaces. To form the BSF and the back electrode, the wafer is flipped and the diffusion of  $p+$  dopants and back metallization are performed, respectively. Figure 2 reveals the proposed structure, which is designed using the Athena fabrication tool. As shown, Figure 2a represents a cross-sectional view of the structure while Figure 2b,c demonstrate cutlines through the vertical and lateral directions, respectively. The doping profiles, including acceptor, donor, and absolute net doping, are shown for the top and the left lateral  $p$ - $n$  junctions.



**Figure 2.** The proposed microstructure generated by Athena process framework (a) cross-sectional view for a unit cell illustrating the absolute net doping, (b) vertical cutline (through  $x = 0 \mu\text{m}$ ) to show the doping profile of the top  $p$ - $n$  junction and (c) lateral cutline (through  $y = 5 \mu\text{m}$ ) to show the doping profile of left  $p$ - $n$  junction.

Next, the structure is simulated by applying the SILVACO device simulator (Atlas) [48]. The first Atlas step simulates the SC response to illumination by the AM1.5 solar spectrum. Based on this illumination, the photogeneration rates are calculated. These rates, upon

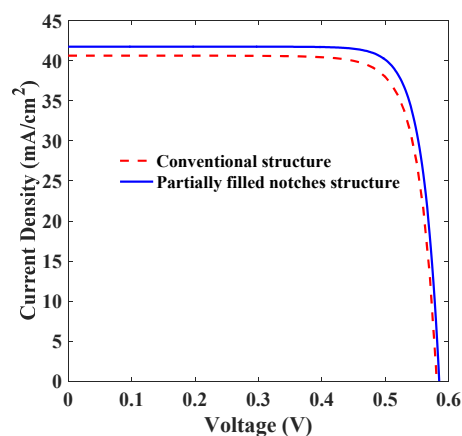
integration, are used as input for the continuity equations. The numerical simulation implemented in Atlas is based on the solution at each mesh point of the basic semiconductor equations, which are Poisson's equation and continuity equations for electrons and holes. These differential equations are iteratively and self-consistently solved by the coupled Newton numerical method to obtain the potential as well as the electron and hole concentrations. Then, the drift-diffusion model is invoked to solve for the transport properties. For these steps to be accomplished, the major physical models necessary for simulation are incorporated. These include mobility models that fulfill concentration and field dependence. The Shockley–Read–Hall (SRH) recombination model is taken to be concentration-dependent. Additionally, Fermi statistics, Auger recombination, and band gap narrowing models are activated to account for the high doping effects. The minority carrier lifetimes of the  $p$ -type base and the  $n$ -type emitter are extracted from the literature [49–51]. For the given design parameters, the bulk lifetime in the base is 5  $\mu\text{s}$ , while in the emitter it is 8  $\mu\text{s}$ .

### 3. Results and Discussion

In this section, we provide the simulation results of the proposed structure. First, we present a comparative study between the partially-filled-notches structure and the conventional one that has completely filled notches, showing the improvement of the presented solar cell inferred from the performance metrics of the solar cells, namely  $J_{sc}$  (short-circuit current),  $V_{oc}$  (open-circuit voltage),  $FF$  (fill factor), and  $PCE$  (power conversion efficiency). Next, applying single, double, and triple ARC configurations, produced efficiency boosting results. A proposed process flow including the design of the front contact is provided, paving the way for the fabrication of the proposed structure.

#### 3.1. Comparison between Partially Filled and Fully Filled Notches Structures

In this subsection, we present a comparative study between the electrical performance of the conventional and the partially-filled-notches npn structure. The comparison is accomplished using the Atlas device simulator. The electrical performance is examined by the illuminated current density—voltage ( $J$ – $V$ ) characteristics under the AM1.5G solar spectrum. Figure 3 shows the characteristics of both structures. A higher short circuit current for the open-notches structure is obvious because the bottom planar solar cell of the open-notches structure is activated compared to the conventional configuration. Furthermore, in Table 1, the extracted electrical performance PV parameters,  $J_{sc}$ ,  $V_{oc}$ ,  $FF$ , and  $PCE$ , are reported for the two structures. As indicated in the table, the  $FF$  of the open notches case is higher than that of the conventional SC. This is due to the lower series resistance [52]. Based on the enhancement of  $J_{sc}$  and  $FF$ , a higher  $PCE$  result regarding the open notches case as it is evident in Table 1. Its efficiency is 0.8% above the conventional cell, which is considered a good enhancement.



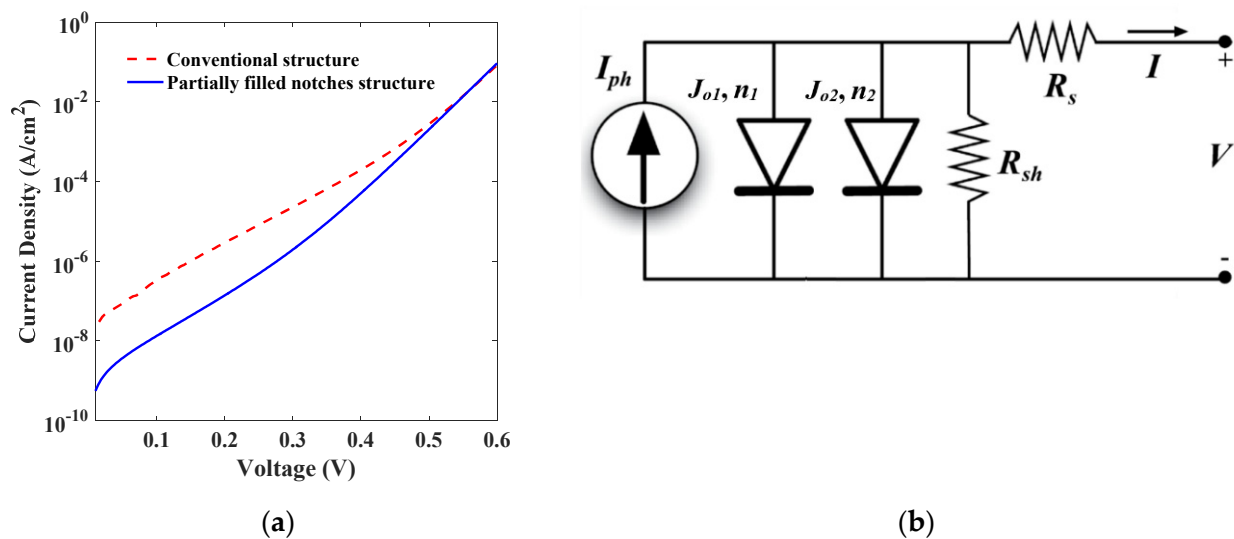
**Figure 3.** A comparison of illuminated  $J$ – $V$  curves between the conventional and partially filled notches structures.



**Table 1.** PV parameters of the conventional and the partially filled notches microstructures.

Structure	$J_{sc}$ (mA/cm <sup>2</sup> )	$V_{oc}$ (V)	FF (%)	PCE (%)
Conventional	40.70	0.580	80.30	14.50
Open notches	41.70	0.582	82.30	15.30

Moreover, the dark characteristics of the two structures are simulated to obtain more physical insight into the differences between them. The simulation results are displayed in Figure 4a. For Si-based SCs, the equivalent circuit of the two-diode model can successfully explain cell behavior. A representation of the circuit is illustrated in Figure 4b. The two main factors describing the diode are the reverse saturation current ( $J_0$ ) and the ideality factor ( $n$ ). Each diode has its own  $J_0$  and  $n$ . The other circuit parameter is the series resistance  $R_s$ . The shunt resistance is assumed to be very large, as is evident from Figure 3. The five parameters are extracted from the dark  $J$ - $V$  curves and are listed in Table 2. Regarding the ideality factor of the first diode, which is effective in the low voltage regime up to 0.4 V, its value regarding the modified structure is less than that of the conventional one, implying less recombination in the bulk region. Regarding the voltage range 0.5 V to 0.6 V, the ideality factor is nearly 1.0, which corresponds to an ideal diode. It might be pointed out here that an ideality factor higher than unity defines the current because of the recombination in the depletion region. On the other hand, a unity value depicts the diffusion current resulting from the recombination in the emitter and base regions of the SC [25].

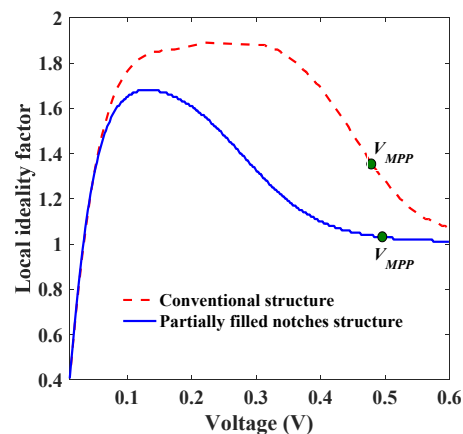
**Figure 4.** (a) A comparison between the dark characteristics of the conventional npn and partially-filled-notches structures and (b) equivalent two-diode model.**Table 2.** Two diode model parameters for the conventional and partially-filled notches microstructures.

Structure	$J_{01}$ (A/cm <sup>2</sup> )	$n_1$	$J_{02}$ (A/cm <sup>2</sup> )	$n_2$	$R_s$ (mΩcm <sup>2</sup> )
Conventional	$3.99 \times 10^{-8}$	1.847	$6.02 \times 10^{-13}$	0.909	6.81
Open notches	$1.24 \times 10^{-9}$	1.713	$7.03 \times 10^{-12}$	1.002	6.76

Although the reverse saturation current of the first diode is lower for the case of the modified structure, the open-circuit voltage of the two structures is nearly the same. This can be explained based on the following analytical equation:

$$V_{oc} \approx n_2 V_T \ln \left( \frac{J_{sc}}{J_{02}} \right), \quad (1)$$

where  $V_T$  is the thermal voltage. While  $J_{o2}$  is lower and  $J_{sc}$  is higher, the value of  $n_2$  is higher for the partially filled structure than for the conventional cell (see Table 2), suggesting a similar  $V_{oc}$  for the two structures. Using Equation (1), the ratio of  $V_{oc}$  of the conventional structure to that of the modified structure is found to be nearly 1.0, which matches the simulation trend. Moreover, to explain the higher  $FF$  obtained from the modified structure over that of the conventional one, the local ideality factor can give a clear view of this change. In this regard, Figure 5 shows the local ideality factor and illustrates the points of  $V_{MPP}$  from which the  $FF$  can be analytically calculated. It has been reported that, as the local ideality factor is higher at  $V_{MPP}$ , for which the maximum output power occurs, a higher  $FF$  occurs [53,54]. This qualitative analysis is in agreement with the recorded values in Table 1.



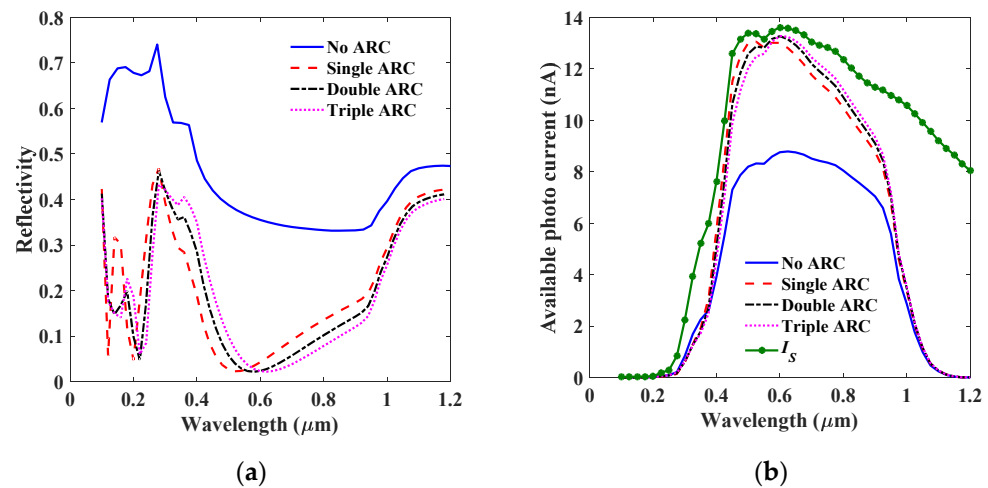
**Figure 5.** A comparison between the local ideality factor, derived from the dark  $J$ - $V$  characteristics, of the conventional and modified structures.

### 3.2. ARC Techniques

In this subsection, the impact of various ARC schemes on the proposed npn SC microstructure performance is investigated. Remarkably, antireflection coating techniques play a crucial role in decreasing the front surface reflectivity. Such techniques could be significantly efficient in enhancing the optical performance of SCs, especially silicon-based cells, due to the high refractive index of silicon [36,37]. Here, single, double, and triple ARC layers are simulated to achieve minimum reflectivity and maximum available photocurrent. As a result, the conversion efficiency will be maximized. The main performance indicators, like reflectivity, as well as available and source photocurrents, are simulated and provided to give a comparative study between the different cases of ARCs.

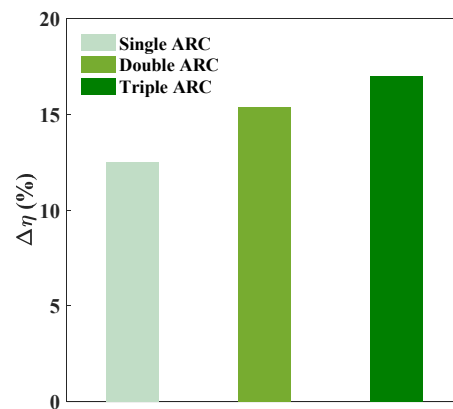
Firstly, the effect of using a single ARC layer of ZnO is carried out. The ZnO is selected as it achieves lower reflectivity in a wider band of the wavelength in comparison with the other single-layer ARCs [55,56]. The thickness of the ZnO ARC single layer is selected to be 64 nm, which is the optimum design condition [55–57]. Secondly, a double ARC layer is chosen for our simulation which is based on the  $\text{Si}_3\text{N}_4/\text{ZnO}$  system. The thickness of the first ARC layer, which is the ZnO, is selected to be 54 nm, while that of the second layer ( $\text{Si}_3\text{N}_4$ ) is selected to be 15 nm. Finally, a triple ( $\text{SiO}_2/\text{Si}_3\text{N}_4/\text{ZnO}$ ) ARC is simulated. The thicknesses of the three layers are selected to be 15, 20, and 50 nm, respectively.

Figure 6 demonstrates the simulation results for the distinct ARC cases. Figure 6a displays the reflectivity behavior, while Figure 6b displays the available photocurrent. The source photocurrent ( $I_s$ ) is also shown for comparison (see Figure 6b). When comparing the case of no ARC with the single layer ZnO ARC, it is obvious that reflectivity is significantly reduced, resulting in a considerable rise in the available photocurrent. The performance metrics for the case of the double ARC technique are better than the single-layer case, as evident from Figure 6 for both reflectivity and available photocurrent above a wavelength of 0.6  $\mu\text{m}$ . Additionally, it is obvious that the triple layer ARC gives the minimum reflectivity and, consequently, better performance of the SC microstructure.



**Figure 6.** Comparison between different ARC methods applied to the proposed structure (a) reflectivity and (b) available and source photo currents.

Moreover, the electrical stimulation of the different ARC methods is performed to extract the *PCE*. The performance indicator regarding this simulation is the relative efficiency  $\Delta\eta$ , which is defined as  $(PCE_{ARC} - PCE_{NoARC})/PCE_{NoARC}$ , where  $PCE_{NoARC}$  and  $PCE_{NoARC}$  represent the efficiency without ARC and when applying ARC, respectively. Figure 7 shows the improvement in the structure conversion efficiency because of the ARC. In the single ARC case,  $\Delta\eta$  is found to be 12.5%, while it is 15.4% for the case of double ARC. In the case of the triple ARC,  $\Delta\eta$  is found to be 17%, which is considered the best performance.



**Figure 7.** Relative efficiency changes utilizing various types of ARC techniques.

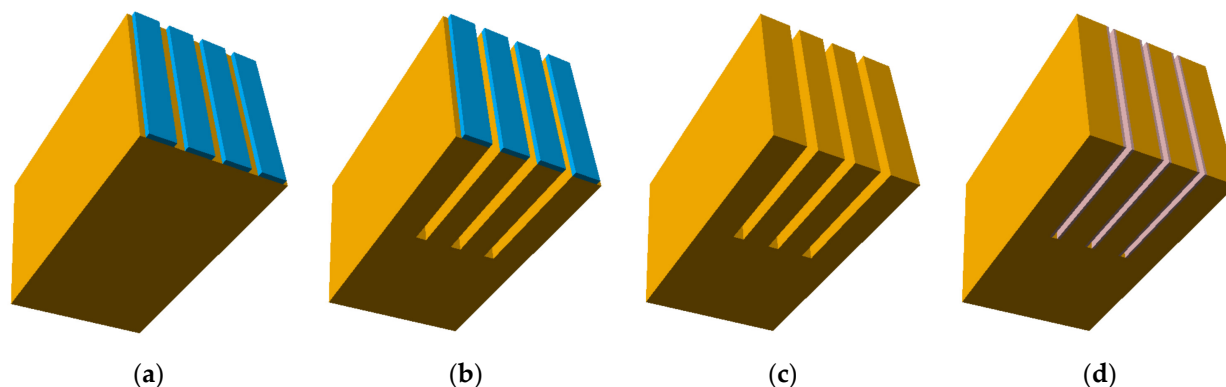
### 3.3. Proposed Process Flow

Concerning the processability of the presented SC, the structure fabrication is straightforward, as it needs the same mature process steps as those encountered in fabricating a conventional planar SC. The extra step is to engrave vertical grooves by generating deep trenches. It is not a challenging or costly additional fabrication step, as the deep trench ion etching (DRIE) process can etch such deep trenches. In addition, the aspect ratio in the structure is 2:75, which is feasible [58].

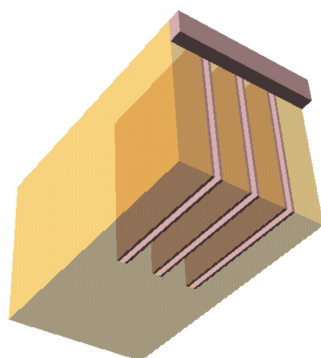
The starting substrate could be chosen to be *p*-type with a high doping level in the order of  $1 \times 10^{18} \text{ cm}^{-3}$ . To prepare for the notches, a periodic photoresist is deposited as strip lines which have a width of  $16 \mu\text{m}$  and a spacing of  $2 \mu\text{m}$ , as illustrated in Figure 8a. Next, to attain a depth of about  $75 \mu\text{m}$ , a deep ion reactive etching is required. This will produce micro-grating notches of  $2 \mu\text{m}$  in width and  $75 \mu\text{m}$  in thickness through the wafer, as represented in Figure 8b. The photoresist layers are then removed by etching, as seen in Figure 8c. The emitter is to be formed using phosphorous atoms at a concentration less than  $5 \times 10^{19} \text{ cm}^{-3}$ , where the junction depth should be less than  $200 \text{ nm}$ . A thickness of



about 100 nm Aluminum (Al) is to be evaporated on the structure, as seen in Figure 8d, utilizing, for instance, an E-beam evaporator. After that, the top Al layer is removed by a commercial tape. The bus-bars connecting all of the emitters are evaporated to form the cathode contact. A thickness of about 500 nm of the Al back electrode is evaporated to form the anode back contact. Finally, the design of the front contact may be done via a bus-bar, like in the case of planar c-Si SC, as displayed in Figure 9. It is noted that the metal penetration for the cathode contact finger helps increase the area, which, in turn, lowers the series resistance. Therefore, the issue of designing the finger width encountered in planar SCs is not faced in our structure.



**Figure 8.** Proposed process flow of the partially-filled notches npn microstructure (a) photoresist deposition, (b) deep etching, (c) after removing photoresist, and (d) after defining side wall emitter contact.



**Figure 9.** 3D schematic representation of the proposed microstructure showing one busbar and finger structure.

It should be pointed out here that plasmonic effects can be produced in such a periodic metallic structure, formed from the finger shape of the proposed structure, as the difference between the electrodes is in the order of  $1\ \mu\text{m}$  [42]. These effects may further support the light coupling into the structure and enhance the performance of the bottom  $p$ - $n$  junction. A detailed study of these effects can be performed in individual future work.

#### 4. Conclusions

In this research work, we introduced a proposed SC structure in which we tried to overcome both electrical and optical losses by properly designing the main cell parameters. The presented npn microstructure is designed in such a way as to alleviate the shadowing effect by opening the deep trenches. The emitter electrode is proposed to be a shallow layer, produced by evaporation for instance, instead of the complete filling of the notches with metal. This design lets the bottom  $p$ - $n$  junction work in the same way as the top junction, implying a higher short circuit current. The performance of the proposed partially-filled-notches microstructure has been compared to that of the conventional cell,

showing an improvement of 0.8% in efficiency. Further, to overcome the light reflections from the surface, we have applied different ARC techniques, namely single, double, and triple systems using ZnO, Si<sub>3</sub>N<sub>4</sub>/ZnO, and SiO<sub>2</sub>/Si<sub>3</sub>N<sub>4</sub>/ZnO. It has been shown, based on simulation results, that there is a relative improvement of 12.5%, 15.4%, and 17% in the efficiency results for the single, double, and triple ARC layers, respectively. Moreover, we have discussed the suggested process flow to fabricate the proposed SC. Finally, we have provided the design of the front contact to achieve minimum electrical and optical losses. The presented study may open a path to the fabrication of a highly efficient SC which is based on low-cost Si wafers.

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